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FINAL REPORT

DEVELOPMENT OF A HIGH EFFICIENCY THIN SILICON SOLAR CELL

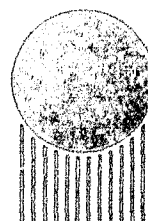
JPL Contract No. 954883

December, 1980

Report No. SX/115/F

By

G. Storti
J. Culik
C. Wrigley



SOLAREX
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SOLAREX CORPORATION
1335 Piccard Drive
Rockville, MD 20850

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Abstract

Technology development is described for high efficiency ultra-thin (50 μm) solar cells. Significant improvements in open-circuit voltage and conversion efficiency, even on relatively high bulk resistivity silicon, are achieved by use of a screen-printed aluminum paste back surface field (BSF). A 4 cm^2 50 μm thick cell was fabricated from textured 10 $\Omega\text{-cm}$ silicon which had an open-circuit voltage of 595 mV and AM0 conversion efficiency at 25°C of 14.3%. The best 4 cm^2 50 μm thick cell (2 $\Omega\text{-cm}$ silicon) produced under this contract had an open-circuit voltage of 607 mV and an AM0 conversion efficiency of 15%. Processing modifications are described which resulted in better front contact integrity and reduced breakage. These modifications were utilized in the thin cell pilot line to fabricate 4 cm^2 cells with an average AM0 conversion efficiency at 25°C of better than 12.5% and with lot yields as great as 51% of starts; a production rate of 10,000 cells per month was demonstrated. A pilot line was operated which produced large area (25 cm^2) ultra-thin cells with an average AM0 conversion efficiency at 25°C of better than 11.5% and a lot yield as high as 17%.

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1. Introduction and Summary

In 1976 Solarex showed that ultra-thin silicon solar cells, 50 μm or less in thickness, could be fabricated in the laboratory.⁽¹⁾ Several hundred of these cells were delivered to the Jet Propulsion Laboratory (JPL) at that time. NASA-OAST, recognizing the importance of this advance in silicon solar cell technology, then directed funding to support pilot line production of these cells under JPL Contract No. 954290. Solarex assembled and began operating a pilot line facility under the above referenced contract in less than three months.⁽²⁾ Cells produced on this pilot line were fabricated from 2 $\Omega\text{-cm}$, p-type, Czochralski-grown silicon wafers thinned by a two-step etching process to the requisite 50 μm thickness. The etch solution was 40% NaOH (by weight) at 110°C. Thinned wafers were then phosphorus-diffused at 865°C for 10 minutes. Ti/Pd/Ag front contacts were applied using photolithographic, rather than shadow-masking techniques. Ta_2O_5 was evaporated as an AR coating and the cells were sintered at 450°C for 1 minute. Figures 1-1 and 1-2 show the yield and AMO power at 25°C vs. lot number in this first exercise of the ultra-thin cell pilot line facility. Yields (AMO output power at 25°C greater than 55 mW) improved considerably during the pilot line operation, increasing to more than 60% by the end of the effort.

Figure 1 - 1

PILOT LINE YIELD

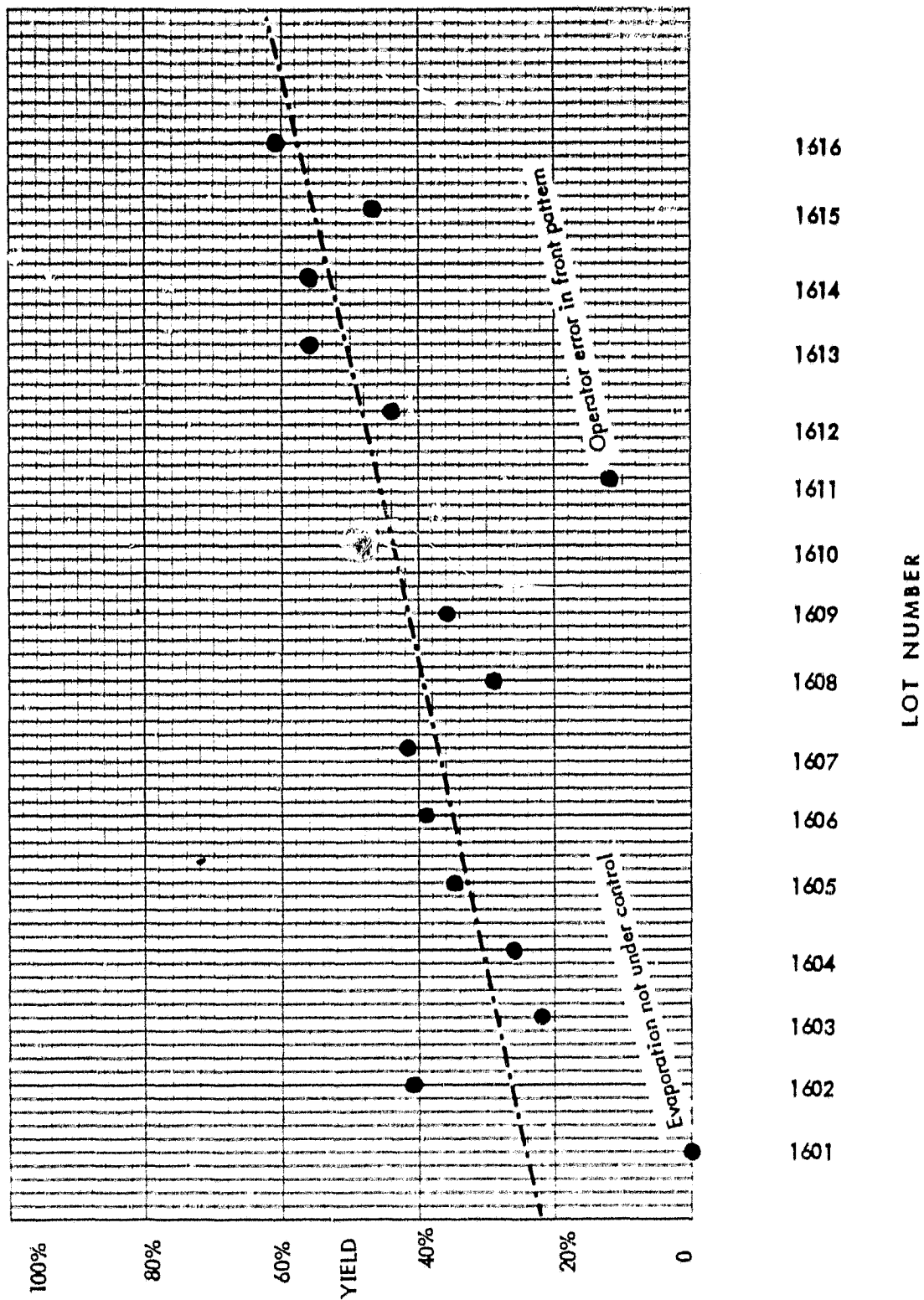
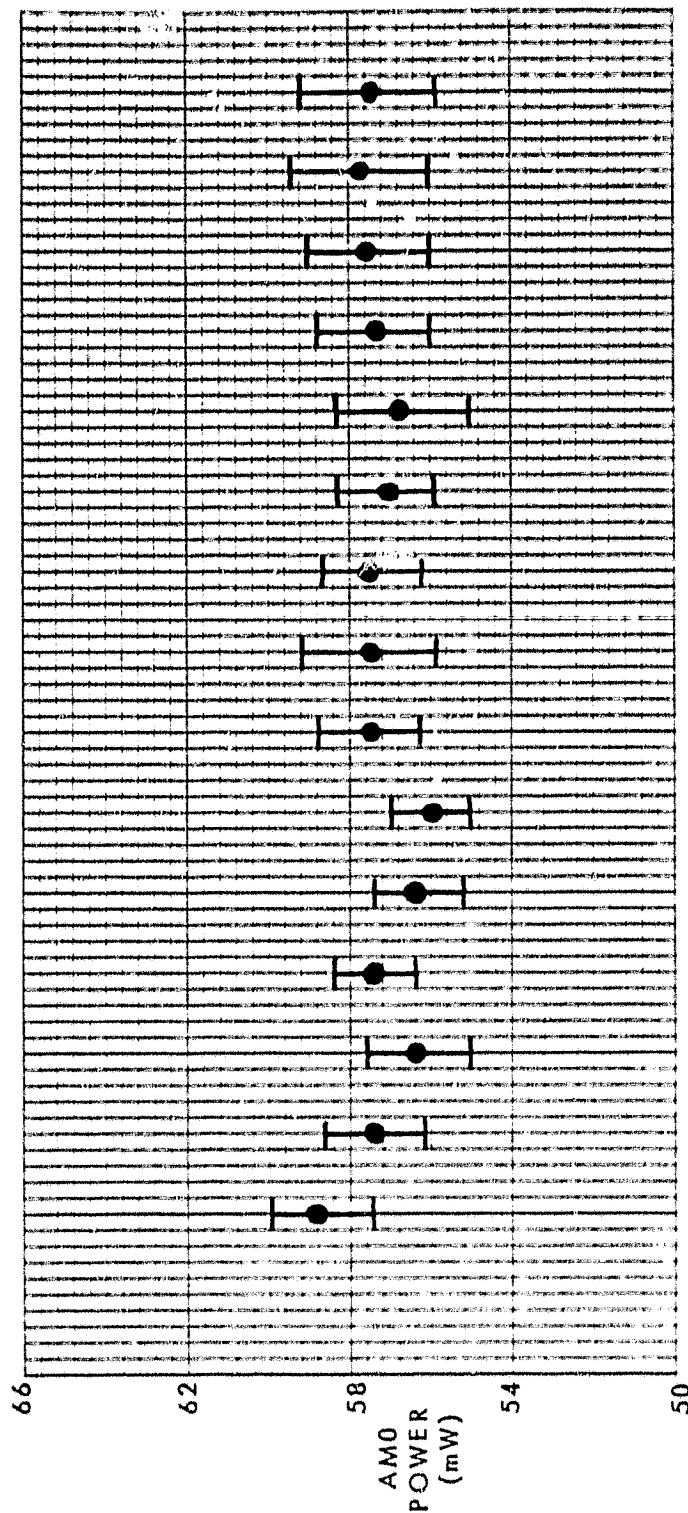


Figure 1 - 2

TWO MIL CELL POWER OUTPUT



Output power remained consistent throughout the pilot line operation, averaging better than 57 mW for a 4 cm² cell. In parallel experimental efforts, 4 cm² cells were fabricated with an output power which exceeded 67 mW.

As a result, the present contract work was started with the principal goals being: (1) to do the necessary research and development that would lead to the production of higher efficiency, thin (25 to 150 μ m thick) silicon solar cells, (2) to fabricate 2000, 2 cm x 2 cm ultra-thin (50 μ m thick) cells in pilot line operations, and (3) to demonstrate a capability for fabricating 4 cm² ultra-thin cells at a 10,000 per month rate. Experimental efforts were to be directed toward improving the silicon thinning process to maximize performance and yield, investigating surface texturing and back surface reflector techniques to improve carrier generation and collection, and developing a technique for back surface field formation to improve the open-circuit voltage characteristic on high bulk resistivity silicon.

Several pilot line runs were made to implement advances in cell technology which were developed during this contract. The first pilot line was operated during the first four quarters of this contract. (3)

A significant increase in average power occurred in the second quarter, primarily as a result of implementing an advance in processing technology. Wafers were tilted in angled-slot diffusion boats so that the front side was convex during the diffusion process (phosphine at 850°C for 15 minutes to a sheet resistivity of 100 - 120 Ω/\square). These cells, like cells fabricated in the previous ultra-thin cell pilot line, had an evaporated aluminum alloy BSF. Yields (AM0 power at 25°C greater than 60mW) for all four quarters were low (not exceeding 35% for any quarter) due to the start-stop nature of the operation and, in the third quarter, to high personnel turnover. However, a production rate of 10,000 4 cm² cells per month was demonstrated. In parallel experimental efforts, cells with AM0 conversion efficiencies at 25°C exceeding 14.5% ($P_{\max} = 79$ mW) were achieved with textured ultra-thin cells. From this work it was clear that the substantial increases in output power could be transferred to cells fabricated on an additional pilot line.

The introduction of the screen-printed aluminum paste alloy technique for the formation of the BSF represented a significant advance over the previous evaporated aluminum alloy technique.⁽⁴⁾ Consequently, a major effort was made in the latter quarters of this contract to develop this technique for use in fabricating high-efficiency ultra-thin cells from relatively high bulk resistivity (7 - 14 Ω -cm) base material.

Achievement of this goal was demonstrated in a second pilot line effort during which more than 2,200 4 cm^2 ultra-thin cells were fabricated in a five-day operation.⁽⁵⁾ These cells were fabricated with an average AM0 conversion efficiency at 25°C of better than 12.5% and with lot yields (AM0 power at 25°C greater than 60 mW) as great as 51% of starts.

This technology was also used in the operation of the first large area (25 cm^2) ultra-thin cell pilot line.⁽⁵⁾ A five-day pilot line effort produced nearly 160 large-area ultra-thin cells with an average AM0 conversion efficiency at 25°C of better than 11.5%. The average yield (AM0 power at 25°C greater than 338 mW) of large-area ultra-thin cells was low because this effort was the first attempt at pilot line production of these cells and a high incidence of wafer breakage was encountered. However, the lot yields improved from only 7% to more than 17% of starts as a result of experience in handling these large-area cells.

In summary, Figure 1-3 shows the work plan and schedule for the research, development and pilot line production efforts to investigate and improve fabrication processes and cell design parameters resulting in high efficiency ultra-thin cells with good yield. The culmination of the research and development efforts was the operation of two pilot lines (in the tenth quarter) - one to produce $2\text{ cm} \times 2\text{ cm}$ ultra-thin ($50\text{ }\mu\text{m}$ thick) cells and one to produce $5\text{ cm} \times 5\text{ cm}$ ultra-thin ($50\text{ }\mu\text{m}$ thick) cells.

Contract Work Schedule (Quarters)

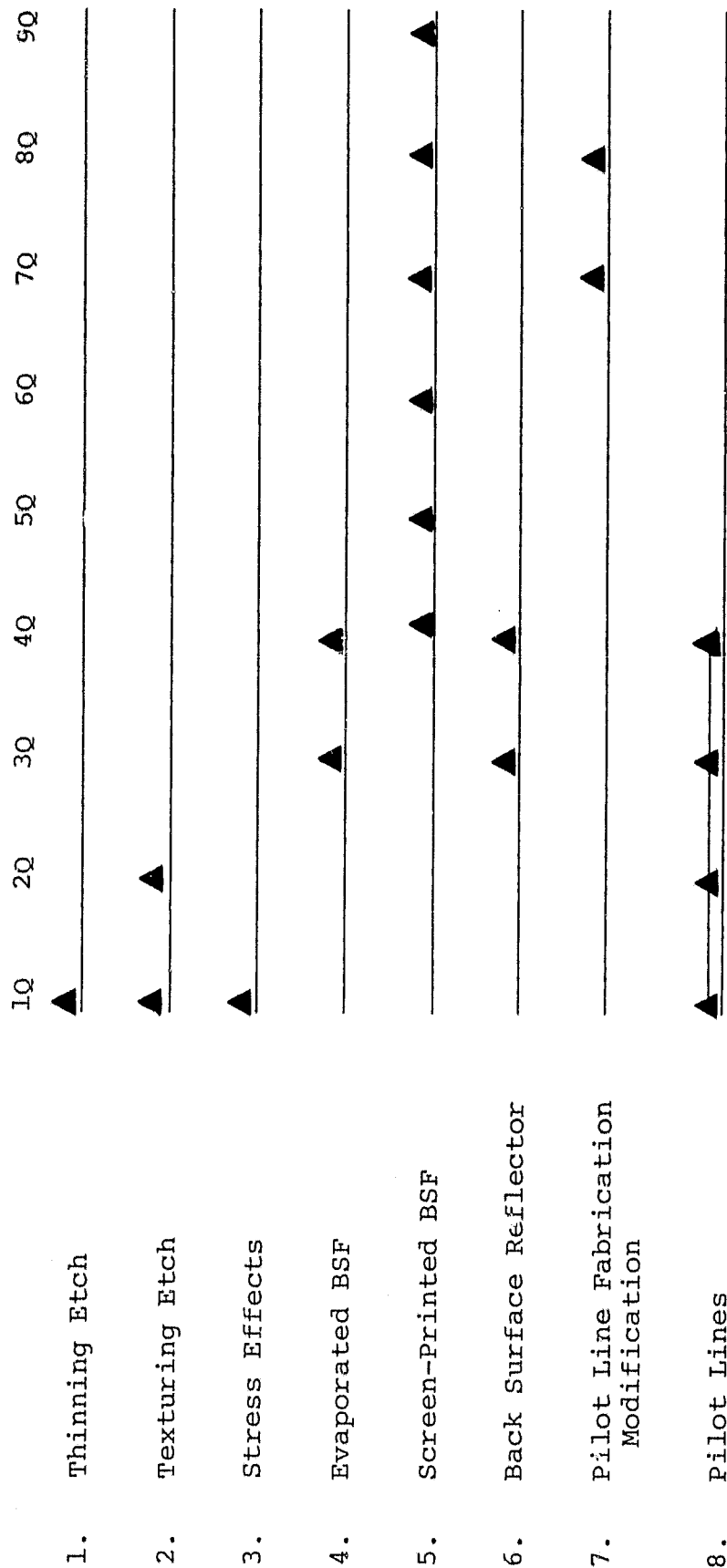


Figure 1-3.

2. Experimental Investigations

Ultra-thin cells produced during the first pilot line effort⁽²⁾ were fabricated from 2 Ω -cm, p-type Czochralski-grown silicon which was thinned to a 50 μ m thickness by a two-step NaOH etching process. Phosphorus diffusions were performed at 865°C for 15 minutes to yield sheet resistivities of 50-70 Ω/\square . The back surface field was developed by alloying 5000 Å of evaporated aluminum at 800°C for 10 minutes into the rear n^+ layer. Front contacts were Ti/Pd/Ag fabricated using photolithographic, rather than shadow masking techniques. A Ta₂O₅ AR coating was evaporated onto the cut cell, which was sintered at 450°C for 1 minute.

Experimental efforts during this contract were directed toward improving the silicon thinning process to maximize performance and yield, investigating surface texturing and back surface reflector techniques to improve carrier generation and collection, modifying the diffusion process to improve performance, and developing a technique for back surface field formation on relatively high (7 - 14 Ω -cm) bulk resistivity silicon. In addition, improvements in ultra-thin cell fabrication were obtained by improving the front metallization integrity and by reducing wafer breakage during processing.

2.1 Thinning Etch

During the previous contract⁽²⁾, it was found that as-sawn wafers of (100) - oriented surfaces could be etched in hot NaOH

solution to thicknesses on the order of tens of microns without selective perforations or thin areas. The thinned wafers had essentially plane, parallel surfaces with a "pillowed" surface microstructure, and were not unmanageably fragile. In this contract, the parameters involved in the etching process were re-examined to determine the optimum conditions for wafer thinning. It was found that the etching process is quite forgiving and that the parameters are reasonably non-critical. Concentrations of NaOH in water ranging from 17% to 40% (by weight) produced essentially identical results if the etchant was kept at a temperature of 105°C or higher. The lower concentration is more economical of materials and produces equally good surfaces and thicknesses, with excellent control. Below 100°C the etch begins to produce square, flat-bottomed preferential indentations in the (100) surface, but this deviation from full-surface planarity disappears completely for etchant temperatures over 105°C. Momentary cooling of the etchant when room-temperatures wafers are placed into the bath is not deleterious when the bath is kept near 110°C, and the incidence of any square-featured indentations then disappears.

While NaOH concentrations as low as 17% by weight are adequate, etching for the Pilot Line cells was performed with a 30% NaOH (by weight) solution in order to insure that the concentration was not depleted by quantity etching.

Wafers were etched to the required 50 μm thickness by a two-step etch process. First, wafers which had been presorted into 7 μm groups (e.g., $300 \pm 3.5 \mu\text{m}$) were etched in the 30% NaOH (110°C) solution to approximately 100 - 125 μm . After determining the batch thickness, and therefore the etch rate, etching was continued until the 50 μm thickness was achieved. Etching action was stopped by quickly placing the thinned wafers into a stop bath of water.

2.2 Surface Texturing

Although wafers which are thinned in the NaOH etchant have a "scalloped" surface topology, a significant improvement in conversion efficiency can be obtained by additional texturing of the front surfaces. The following procedure was found to result in nearly 100% packing density of (111) pyramids. First, (100) - oriented wafers which have been thinned by the NaOH etch are placed into a 4% (by weight) KOH water solution. The solution is brought up to 80 - 85°C at which time isopropyl alcohol (10% by volume) is added to the solution. The slices are kept in the solution for 15 minutes at temperature, removing approximately 15 to 20 μm of thickness.

In one particular experiment to compare the effect of texturing, the short circuit current density increased by 6 to

8 percent as a result of texturing the surface. The difference in current density is largely due to reduced reflection from the textured cells. Figure 2-1 shows the spectral dependence of the reflectivity of two high-current cells, one un-textured ($J_{sc} = 37.5 \text{ mA/cm}^2$) and the other textured (40.8 mA/cm^2). It is clear that texturing widens the low reflectivity region, although it does not decrease the minimum reflectivity. Integrating over the useful AMO spectrum (400 to 1000 nm), the absorptance increases from 87% to 91% as a result of texturing. In addition, the texturing enhances the cell response at the longer wavelengths ($\lambda \geq 800 \text{ nm}$), as shown by Figure 2-2 in which the quantum yield is plotted as a function of wavelength. This result is most likely attributable to the generation of minority carriers nearer the junction because the entering light is deviated from its normal incidence by the textured surface. Absorption/generation then occurs closer to the junction and results in an increased quantum yield.

Open-circuit voltages have shown a substantial variation that is independent of expected effects from texturing - i.e., texturing should increase the junction area, decrease the light-generated current density, and thereby decrease the open-circuit voltage. The increase in junction area is seen in the increased junction capacitance of textured cells (Table 2-1). However, the open-circuit voltage of the most highly textured cell is the highest of the three. Consequently,

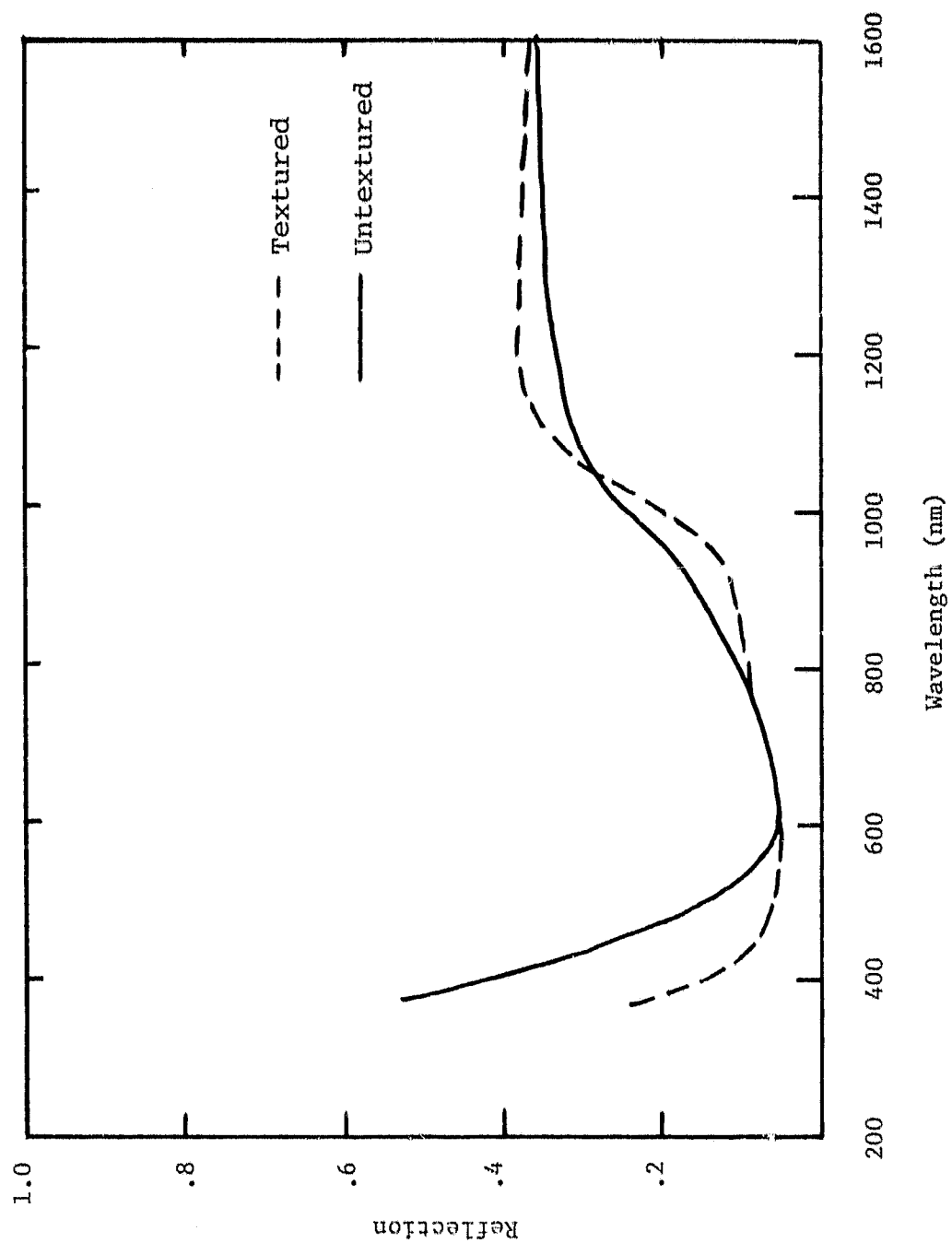


Figure 2-1. Spectral dependence of the reflectivity of untextured and textured 2cm x 2cm cells (without coverslides).

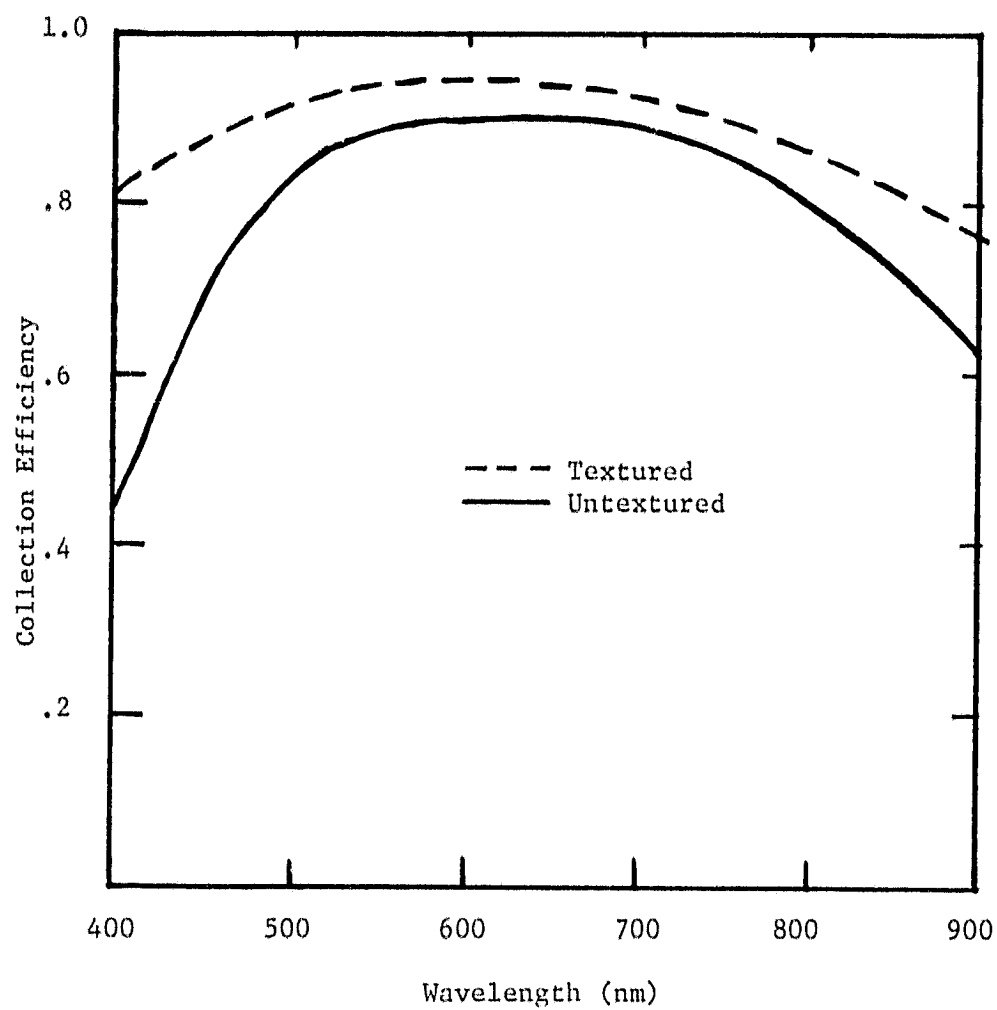


Figure 2-2. Spectral dependence of the collection efficiency of untextured and textured 2cm x 2cm cells (without coverslides).

Table 2-1

COMPARISON OF DARK CAPACITANCE AND V_{oc}

Cell #	C_{dark} (V=0)	Area Factor	V_{oc} (mV)	Comments
I	107 nF	1	569 mV	Untextured
2806-1	140 nF	1.3	568 mV	Partial Texture
2810-3	192 nF	1.8	578 mV	Full Texture

it appears that texturing had no significant effect on the open-circuit voltage of these cells.

2.3 High Temperature Stress Effects

A significant improvement in ultra-thin cell performance was obtained in the first quarter of this contract by diffusing etched wafers such that the front surface was convex. Pilot line cells fabricated without stressed fronts had output powers which averaged 59 mW. Application of stress while diffusing improved the output power to nearly 63 mW.

Since 50 μm wafers tend to bow of their own weight when not lying on a horizontal surface, they are very likely to be stressed during high temperature processing steps such as diffusion and BSF alloy. Investigation of the effect of stress on the performance of ultra-thin cells was performed by diffusing wafers which were purposely stressed. This was accomplished by placing thinned wafers in quartz boats which had wafer-holding slots cut at 45° from the vertical. The wafers were then bowed by their own weight. Half of the wafers were diffused with their front surface convex; the other half had concave-stress fronts. The diffusion was performed with phosphine at 840°C to yield a sheet resistivity of 115 - 135 Ω/\square . The BSF was formed by alloying 8000 \AA of evaporated aluminum at

840°C with the wafer oriented with the same direction of curvature as for the diffusion. The results are shown in Table 2-2. There is a significant improvement in cell output power when wafers are stressed so that the front is convex during high temperature processing. Both the open-circuit voltage and the short-circuit current increased as a result of convex-front stress, indicating that this orientation creates less damage to the silicon lattice. All subsequently fabricated cells with evaporated aluminum BSF's were processed so that the front was convex-stressed.

2.4 Back Surface Fields

One of the tasks of this program was to develop techniques which would consistently yield good back surface fields (BSF) and improved open-circuit voltages, especially on relatively high bulk resistivity (approximately 10 Ω -cm) silicon. Initial efforts dealt with techniques of fabricating the BSF with evaporated aluminum layers, while later work was concerned with screen-printed aluminum BSF's. For the sake of completeness, experimental results on both techniques are presented. It should be noted, however, that the screen-printed BSF gives consistently superior results.

Table 2-2

Effect of Concave and Convex Stress on Cell Performance
(N = 240 cells)

1. Concave Front

$$\bar{V}_{oc} = 568 \text{ mV}$$

$$\bar{J}_{sc} = 135 \text{ mA}$$

$$\bar{P} = 59 \text{ mW}$$

2. Convex Front

$$\bar{V}_{oc} = 574 \text{ mV}$$

$$\bar{J}_{sc} = 145 \text{ mA}$$

$$\bar{P} = 65 \text{ mW}$$

2.4.1 Evaporated Aluminum BSF

It was considered that the thickness of the evaporated aluminum layer could affect the open-circuit voltage produced by the ultra-thin cells. Consequently, aluminum was evaporated at two different thicknesses, 1 and 2 μm , then alloyed for a very short time (approximately 30 seconds) at 1050°C. The results are shown in Table 2-3. Typical cells had AMO output powers exceeding 70 mW; the best cells had an output power of 77 mW. With respect to performance, there was not that much difference between the 1 μm and 2 μm thick evaporated aluminum layers. The open-circuit voltages were between 565 and 585 mV; the current density varied from 38.8 to 41.5 mA/cm². However, a higher incidence of junction shunts was observed in cells on which 2 μm of aluminum had been evaporated, primarily because aluminum had locally agglomerated and alloyed through to the front of the wafer. The results of Table 2-3 show, and additional experiments confirmed, that the surface morphology of the back -- textured or non-textured -- does not have significant influence on the output power or the current density. However, it was subsequently found that alloying evaporated aluminum into a textured back surface results in a better BSF more often. Table 2-4 summarizes data on a lot of 55 textured cell which were fabricated with 7000 Å of evaporated aluminum alloyed at 920°C. The best cell had an AMO conversion efficiency (at 25°C) of

Table 2-3

Performance Characteristics of Textured Cells with an Evaporated Aluminum BSF Alloyed at 1050°C (2 Ω -cm silicon).

1. Untextured Back; 1 μ m Aluminum

(N = 5 cells)

V_{oc}	=	577 mV
V_{oc} (max)	=	535 mV
I_{sc}	=	162 mA
I_{sc} (red)*	=	78 mA
I_{sc} (blue)**	=	52 mA
P	=	74 mW

2. Textured Back; 1 μ m Aluminum

(N = 4 cells)

V_{oc}	=	565 mV
V_{oc} (max)	=	569 mV
I_{sc}	=	156 mA
I_{sc} (red)	=	74 mA
I_{sc} (blue)	=	53 mA
P	=	70 mW

3. Untextured Back; 2 μ m Aluminum

(N = 4 cells)

V_{oc}	=	566 mV
V_{oc} (max)	=	566 mV
I_{sc}	=	163 mA
I_{sc} (red)	=	80 mA
I_{sc} (blue)	=	51 mA
P	=	71 mW

4. Textured Back; 2 μ m Aluminum

(N = 4 cells)

V_{oc}	=	573 mV
V_{oc} (max)	=	578 mV
I_{sc}	=	162 mA
I_{sc} (red)	=	80 mA
I_{sc} (blue)	=	51 mA
P	=	70 mW

*Corning Filter #2408

**Corning Filter #9788

Table 2-4

Performance Characteristics of Textured Cells Fabricated
with an Evaporated Aluminum BSF Alloyed at 920°C.

Sample Size: 55 cells

Evaporated Al BSF

Textured 2 Ω -cm

Alloy at 920°C

\bar{V}_{oc}	=	581 mV
\bar{I}_{sc}	=	171 mA
$\bar{I}_{sc}(\text{red})^*$	=	87 mA
$\bar{I}_{sc}(\text{blue})^{**}$	=	52 mA
\bar{P}	=	75 mW
η	=	13.9%

*Corning Filter #2408

**Corning Filter #9788

14.7% (19.9 mW/cm^2). However, several cells processed with this lot were badly shunted due to localized balling up of the aluminum during alloy. This problem was all but eliminated when screen-printed BSF's were used.

2.4.2 Screen Printed Aluminum Paste BSF

) Since the screen-printed BSF was potentially an inexpensive, quick, and reliable method of obtaining high open-circuit voltage, a major commitment was made in this contract to develop this technique to give consistently good quality BSF's on 10 to 25 $\Omega\text{-cm}$, 50 μm thick wafers.

One of the earliest experiments directed toward achieving high efficiency ultra-thin cells using screen-printed aluminum was concerned with the effect of paste consistency on open-circuit voltage. Englehard A3484 aluminum paste of two consistencies was screen-printed onto the textured backs of diffused wafers. One consistency was that as obtained from Englehard and the other was that which resulted by adding an equal amount of thinner. The pastes were not baked prior to being inserted into a furnace at 850°C . Flaming of the organic vehicle occurred, and the wafers were removed after approximately 30 seconds. The results are seen in Table 2-5. They show very clearly that the thicker consistency paste gives higher open-circuit voltages.

Table 2-5

Effect of Aluminum Paste Thickness on Open-Circuit Voltage

1. Thick consistency paste (no dilution)

(N = 5 cells)			
\bar{V}_{oc}	=		561 mV
V_{oc} (min)	=		549 mV
V_{oc} (max)	=		570 mV

2. Thin consistency paste (1 part paste, 1 part thinner)

(N = 12 cells)			
\bar{V}_{oc}	=		508 mV
V_{oc} (min)	=		503 mV
V_{oc} (max)	=		512 mV

A companion experiment was directed towards determining the effects of baking the paste at a low temperature prior to alloying. One group of cells was alloyed with no prior curing and another group was baked at 90°C for 10 minutes before alloying at 850°C for 30 seconds. The results of this experiment are seen in Table 2-6. The results clearly show that baking the paste before alloying gives higher open-circuit voltages.

Stress and temperature gradients during alloying were found to have a significant effect on the open-circuit voltage and power of thin cells. In one experiment, the orientation of the wafer was varied. The wafers were placed flat on a boat with the paste layer either up or down. The results, shown in Table 2-7, indicate that alloying the aluminum paste with the layer down, in contact with the boat, results in significantly degraded open-circuit voltages.

Several experiments were performed to investigate the effect of alloy temperature on open-circuit voltage. Diffused textured wafers with a layer of Englehard A3484 aluminum paste were alloyed at 700°C, 750°C, 800°C, 850°C, 900°C and 1000°C. The paste was baked at 90°C for 30 minutes to remove the volatile solvents and to prevent ignition and blistering. The tube entry, alloy and exit times were set at 30 seconds, 30 seconds, and 60 seconds, respectively, for all alloy tem-

Table 2-6

Effect of Baked or Wet Aluminum Paste on Open Circuit
Voltage.

1. Alloying of baked paste.

(N = 30 cells)

\bar{V}_{oc}	=	582 mV
V_{oc} (min)	=	556 mV
V_{oc} (max)	=	595 mV

2. Alloying of wet paste

(N = 17 cells)

\bar{V}_{oc}	=	566 mV
V_{oc} (min)	=	551 mV
V_{oc} (max)	=	577 mV

Table 2-7

Effect of Wafer Orientation during Alloying on Open-
Circuit Voltage

1. Wafer Flat, Paste Side Up

(N = 14 cells)			
\bar{V}_{oc}	=		578 mV
V_{oc} (min)	=		551 mV
V_{oc} (max)	=		591 mV

2. Wafer Flat, Paste Side Down

(N = 20 cells)			
\bar{V}_{oc}	=		568 mV
V_{oc} (min)	=		533 mV
V_{oc} (max)	=		580 mV

peratures. The results are shown in Table 2-8. No wafers survived the 1000°C alloy because of breakage associated with severe cell warpage and aluminum locally alloying through the cells. The variation of the open-circuit voltage and the short-circuit current with alloy temperature for the remaining wafers is shown in Figure 2-3.

The open-circuit voltage appears to reach a maximum value at an alloy temperature of 850°C, and is lower at either lower or higher temperatures. The best open-circuit voltage of 596 mV was obtained for an 850°C alloy. However, further experience with aluminum paste BSF's has shown that alloy temperatures from 800°C to 850°C give similar results. Alloy temperatures below 850°C do not have much effect on the short-circuit current. However, the short-circuit current is substantially lower for cells alloyed at 900°C. This degradation may be due to the diffusion of lifetime-killing impurities, such as iron which is known to be a constituent of the paste, at the higher temperature.

The relationship between alloy time and temperature was investigated by alloying similarly screen-printed wafers at two temperatures -- 800°C and 875°C -- with the following program: (1) thirty seconds entry time, thirty seconds at temperature, and rapidly withdrawn; (2) thirty seconds entry time, sixty second at temperature, and rapidly withdrawn; and (3) thirty seconds entry time, ninety seconds at temperature, and rapidly withdrawn. The results for the two alloy temperatures are seen in Table 2-9.

Table 2-8

Dependence of the Open-Circuit Voltage and Short-Circuit
Current on Aluminum Paste Alloy Temperature

	Alloy Temperature (°C)					
	700	750	800	850	900	1000
N (cells)	5	16	30	34	10	--
\bar{V}_{oc}	545	557	564	578	567	--
V_{oc} (max)	563	581	581	596	580	--
V_{oc} (min)	536	533	523	553	542	--
\bar{I}_{sc}	152	154	155	156	148	--

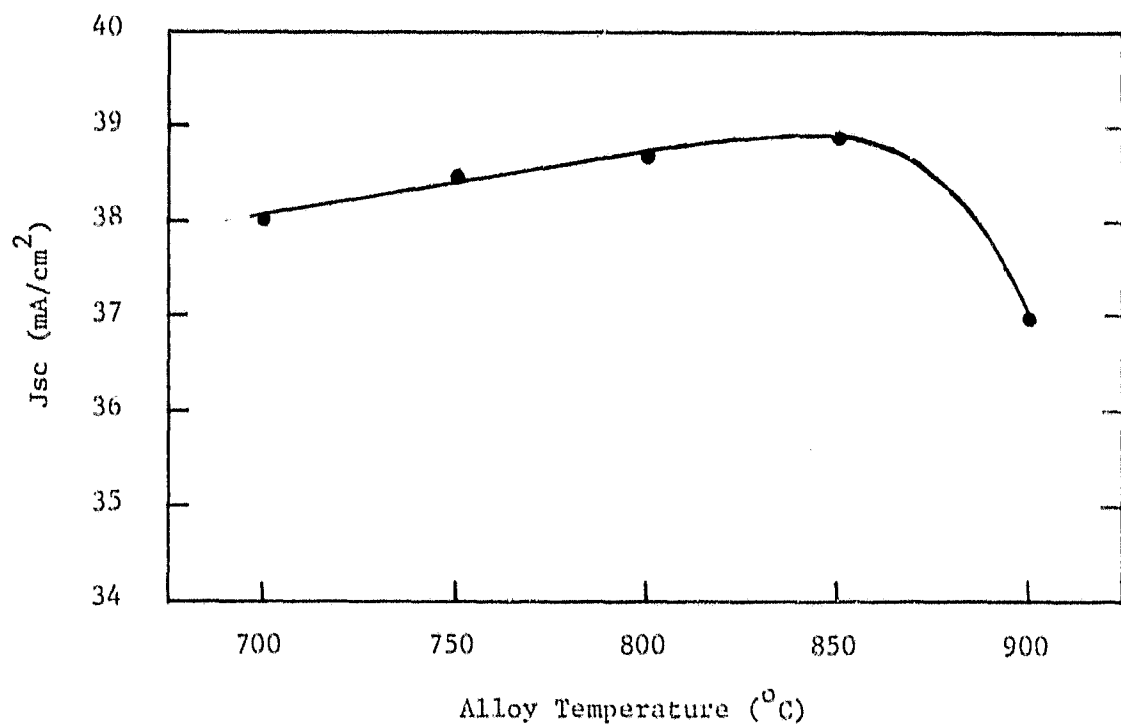
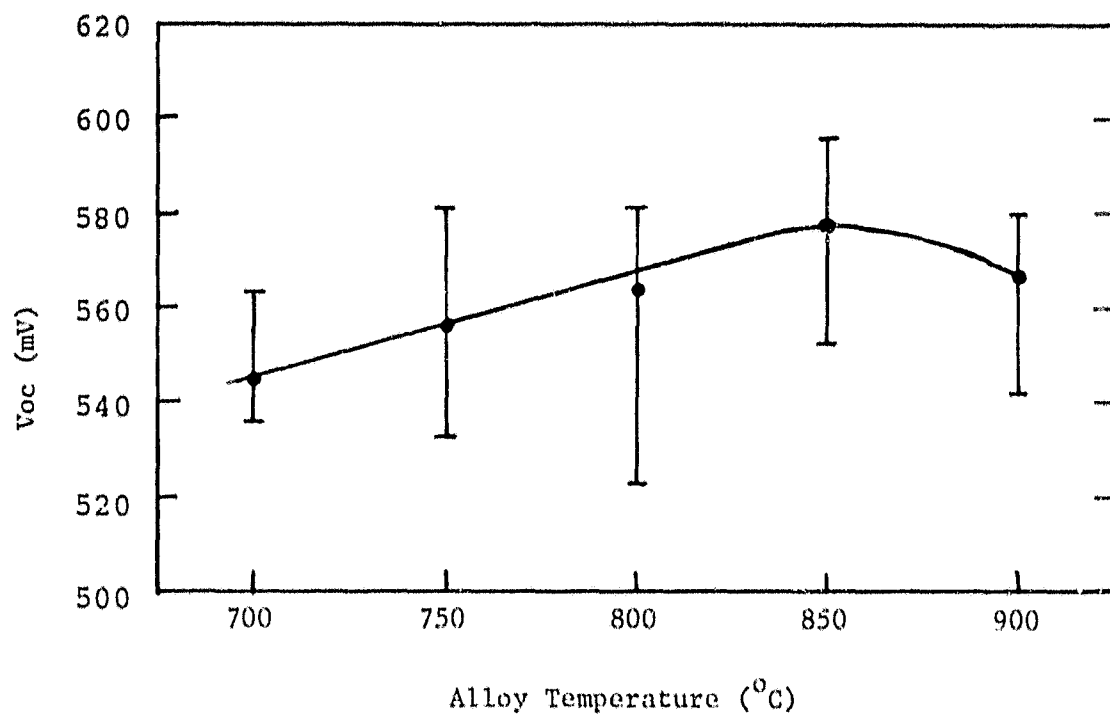


Figure 2-3. Variation of V_{oc} and J_{sc} with Alloy Temperature. (AMO, 25°C)

Table 2-9

Influence of Alloy Time on Cell Output
 Characteristics for Alloy Temperatures
 of 800°C and 875°C

T_{Alloy}	Entry Time/Alloy Time	# of Cells	\bar{V}_{OC} (mV)	\bar{I}_{SC} (mA)	\bar{P} (mW)
800°C	30 sec/30 sec	25	584	156	70
800°C	30 sec/60 sec	27	588	160	71
800°C	30 sec/90 sec	18	586	156	68
875°C	30 sec/30 sec	11	578	157	67
875°C	30 sec/60 sec	11	563	155	67
875°C	30 sec/90 sec	20	556	152	64

For an alloy at 800°C, there is relatively little variation in cell open-circuit voltage, short-circuit current or power with time in the alloying tube, although a 60 second residence time gave somewhat better results. However, for the alloy at 875°C, the shorter residence times resulted in higher cell outputs. Both the open-circuit voltage and the short-circuit current decreased significantly with alloy time. This suggests that diffusion of impurities is not significant at 800°C, while this lifetime degrading process is occurring more rapidly at somewhat higher temperatures.

Entry time, the time it takes to move the boat from the tube entrance to the hot zone, was also found to affect output performance. Entry times of fifteen seconds and forty-five seconds were chosen, and both groups were held at 825°C for forty-five seconds before being rapidly withdrawn. The results are seen in Table 2-10. The fifteen second entry time groups showed a higher average open-circuit voltage and a slightly higher short-circuit current.

From the results of the above described experiments, it appears that the more rapidly the alloy process is accomplished, the higher the cell performance. As a consequence, subsequent alloying was performed at 825°C with minimal entry, residence and withdrawal times.

Table 2-10

Influence of Entry Time on Cell Output
Characteristics for an Alloy Temperature
of 825°C

Entry Time/Alloy Time	# of Cells	\bar{V}_{OC} (mV)	\bar{I}_{SC} (mA)	\bar{P} (mW)
15 sec/45 sec	19	594	163	74
45 sec/45 sec	24	588	162	72

Throughout the experiments on screen-printed aluminum alloy BSF's, the wafers were always found to curl after alloying although the amount varied from batch to batch. Badly curled wafers gave very low yields due to breakage in the wafer cassettes during the alloy clean-up. The warping is apparently due to the different thermal expansion coefficients of silicon and aluminum. After alloying and cool-down a continuous layer of aluminum exists on the silicon, and the thickness of this layer determines the degree of warpage. This idea is further reinforced by the fact that etching the unalloyed aluminum (after alloying) allows the wafers to relax to the point that little warpage exists.

A number of experiments were performed to determine the critical screen-printing parameters that affect the warpage of the thin silicon wafers. To test the effect of screen mesh size on warpage, a lot of wafers was screen-printed with Englehard 3484 paste using 100, 150, and 200 mesh screens. All other screen-printer parameters were held constant. All of the wafers were baked for 20 minutes, then alloyed at 850°C for 25 seconds using a rapid entry and withdrawal.

HCl (100%) was used to remove the excess aluminum after alloying. All eight wafers printed with the 100 mesh screen were too warped to process. Microcracks were observed in the curl

direction, and the wafers tended to disintegrate when handled. Those wafers printed with the 150 mesh screen were very warped. While alloy clean-up was attempted by processing these in round carousels, none survived the HCl etch. However, all eight 200 mesh printed wafers were cleaned with 100% yield.

In a second experiment, 200 and 250 mesh screens were used to print the aluminum paste. A 21% breakage out of 80 wafers was obtained for the 200 mesh screen. An 8% breakage out of 75 wafers resulted with the 250 mesh screen.

2.5 Back Surface Reflector

Early experiments on cells with evaporated aluminum BSF's indicated that the short-circuit current was high even though the reflectivity from the back surface was low. Figure 2-4 shows the reflectivity as a function of wavelength for high efficiency cells having both textured and untextured backs. The reflectivity for both remains at less than 20% even for long wavelengths. A significant improvement in the reflectance of the back surface was obtained by improving the clean-up of the alloy residues using an HCl etch followed by an ultrasonic water rinse. Figure 2-5 shows the reflectivity versus wavelength of two high efficiency cells, one which was cleaned only in the HCl etch, and the other which was cleaned

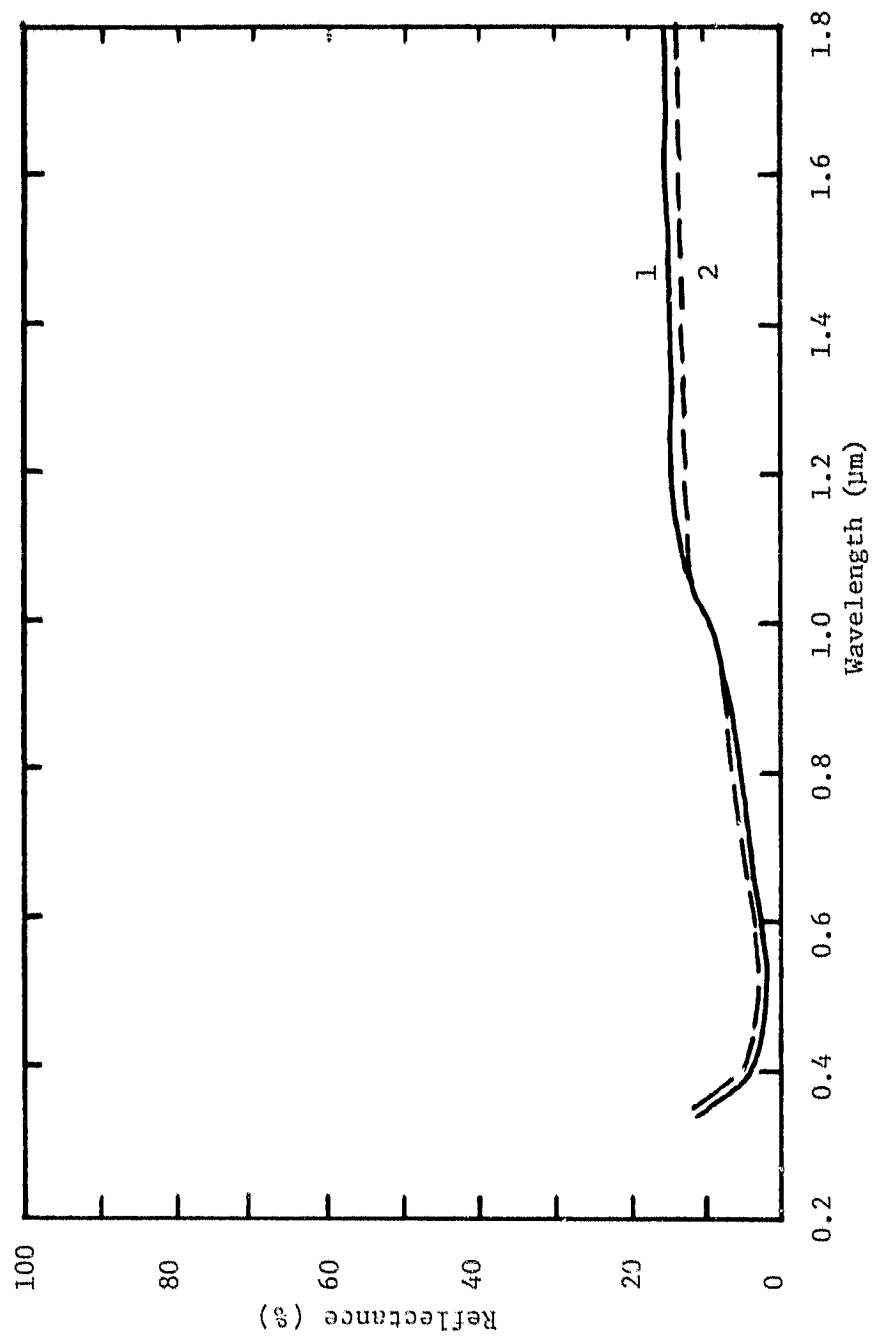


Figure 2-4. Spectral Dependence of the Reflectance for ultra-thin Cells.
with 1) Textured Back and 2) Untextured Back.

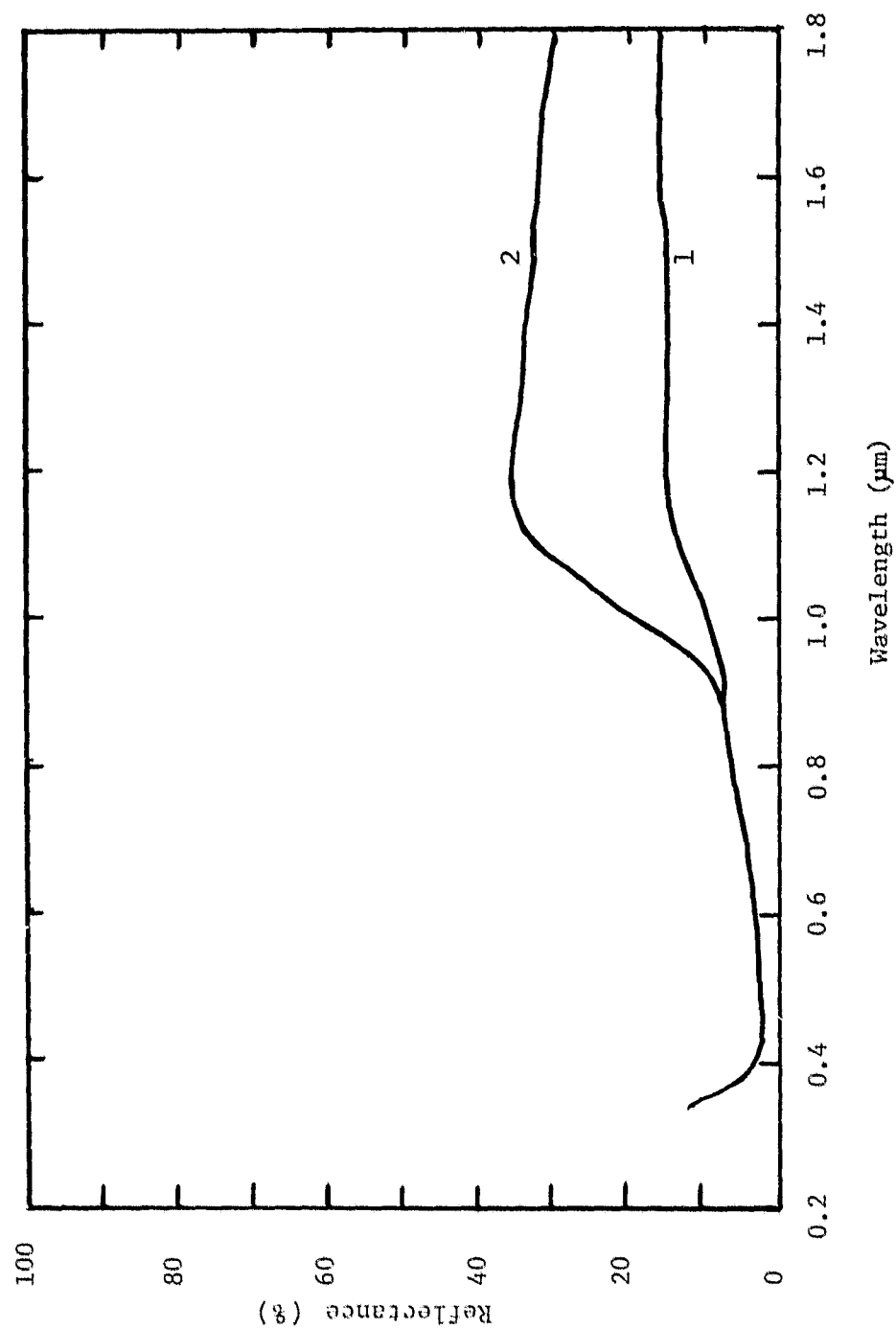


Figure 2-5. Spectral Dependence of the Reflectance for Ultra-Thin Cells with Textured Backs.
 1) HCl Etch Only, 2) HCl Etch with Ultrasonic Cleaning.

with the etch and an ultrasonic water rinse. The internal reflectance at the back has increased from approximately 15% to better than 30% with titanium directly on the silicon. The improved etch/rinse step appears to remove a thin but strongly absorbing layer of alloy residues. This clean-up procedure was subsequently used in the fourth quarter pilot line effort. After the change to aluminum paste BSF's, an essentially equivalent clean-up procedure was used. No further attempts to improve back surface reflectance were made during the contract although the reflectance would be increased by evaporating a fresh layer of aluminum onto the back surface after alloy clean-up and prior to back surface metallization.

2.6 Ultra-Thin Cell Fabrication Process Changes

Since front contact metallization integrity is a very important aspect of ultra-thin cell processing, a substantial effort was made toward increasing metallization adherence. The improvements in the contact integrity are due to changes in wafer processing at the photolithographic, metal evaporation, and plating steps. First, a previously used HF etch step after photolithographic pattern development and prior to the front Ti/Pd evaporation was omitted. Removal of the thin thermal oxide between the metallization and the front surface is unnecessary since sintering results in good electrical contact through the

oxide. Second, increased exposure time yielded wider front metallizations, which further improved adhesion. And finally, introduction of a low temperature heat treatment (150°C for 20 minutes) after the front Ti/Pd evaporation and prior to silver plating resulted in better contact integrity. Very few high-efficiency 4 cm² ultra-thin cells produced by the tenth quarter pilot line failed the standard tape peel test, indicating the efficacy of the procedures.

Breakage of wafers during processing was reduced by the following changes: (1) at the screen-printing step, a new vacuum chuck was designed and fabricated which held the wafers more securely and uniformly; (2) the screen-printer was adjusted to produce thinner paste layers resulting in less warped wafers after alloying, which reduced breakage during the alloy clean-up; (3) at the photoresist spin-on step, the wafers were cushioned on the chuck by a plastic film which minimized the effects of lumps left from the Al alloy; and (4) the plating racks were redesigned to improve the wafer hold-down (steel racks with magnetic hold-down) and minimize silver build-up.

It should be noted that there are some trade-offs to cell performance associated with several of these changes. Longer exposure times will improve the front contact adhesion, but at the expense of reduced current density and conversion efficiency due

to increased shadowing by the metallization. And while thinner paste layers will reduce wafer warpage and therefore breakage, thin paste layers were also found to result in lower open-circuit voltages. This appears to be due to the formation of voids in the alloyed layer due to the thinness of the screen-printed paste layer.

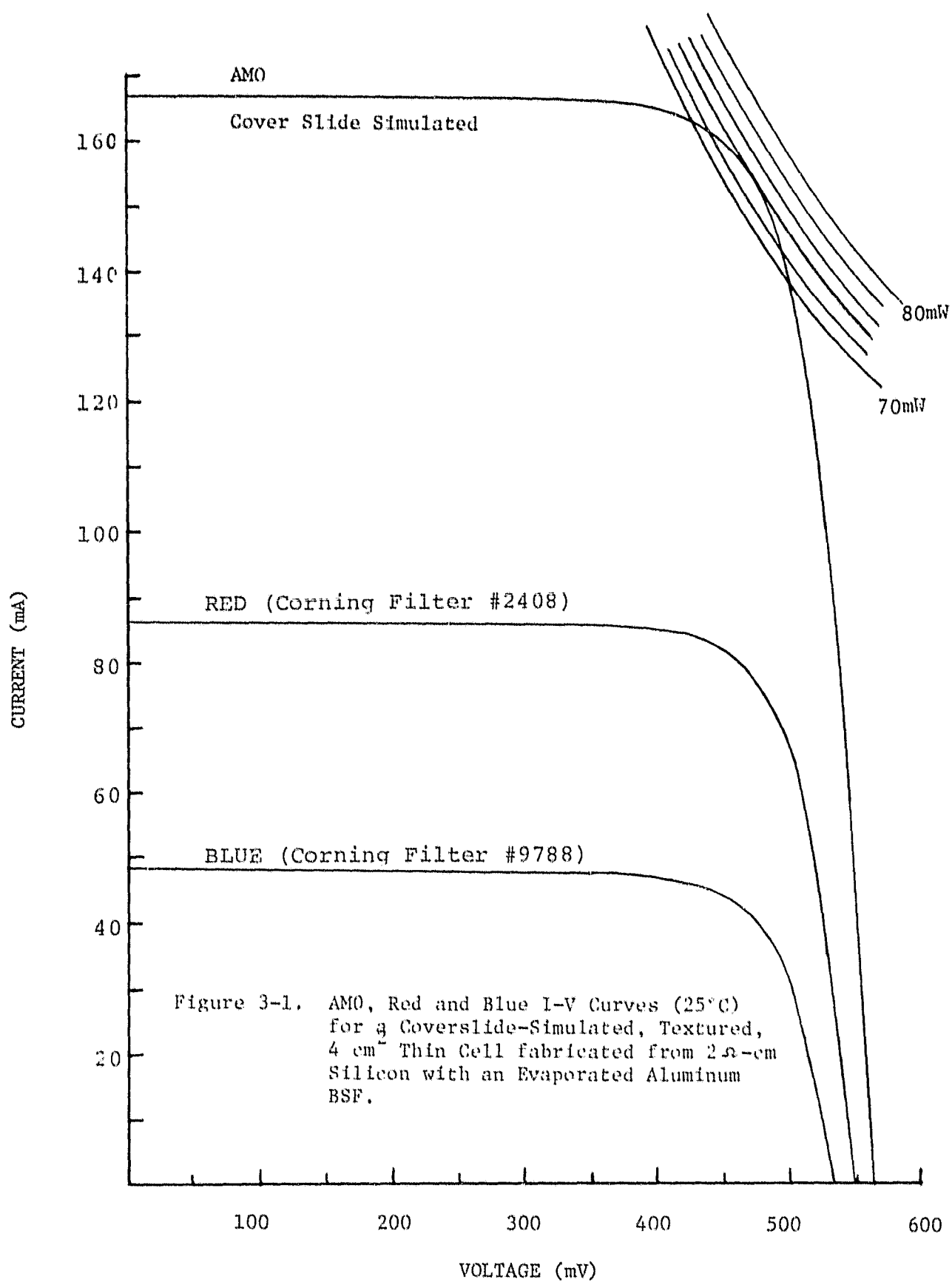
The effect of these improvements in contact integrity and yield of pilot time line cells is discussed in section 4.

3. High Efficiency Ultra-Thin Cells

A major emphasis in the contract was to increase the efficiency of the cells being fabricated on the pilot lines. Consequently, considerable efforts were expended in the laboratory to fabricate the highest efficiency cells possible using techniques that were transferable to the pilot line. All cells fabricated in these efforts were textured in order to maximize the optical coupling.

For the first year of the contract, evaporated aluminum was used as the source for back surface field formation. Also, 2 Ω -cm p-type silicon was used. Initially, the best 4 cm² ultra-thin cell that was fabricated had an AMO power density of 18.3 mW/cm² (Figure 3-1) with a short-circuit current density (J_{sc}) of 41.8 mA/cm² and open-circuit voltage (V_{oc}) of 565 mV. In subsequent experiments, it was possible to increase the power density of the best cell to 19.9 mW/cm² with a J_{sc} of 42.5 mA/cm² and V_{oc} of 594 mV. (Figure 3-2). However, power densities decreased significantly when higher base resistivity material was used.

Because of the success reported with aluminum paste for the source of back surface fields, particularly on higher base resistivity material used for space cells, all subsequent experimental efforts utilized aluminum paste supplied by Englehard Industries. Figure 3-3 shows the I-V characteristics of the best cell fabricated from ~ 10 Ω -cm material. The power density of the cell was 19.3 mW/cm² with a J_{sc} of 41.5 mA/cm² and V_{oc} of 595 mV.



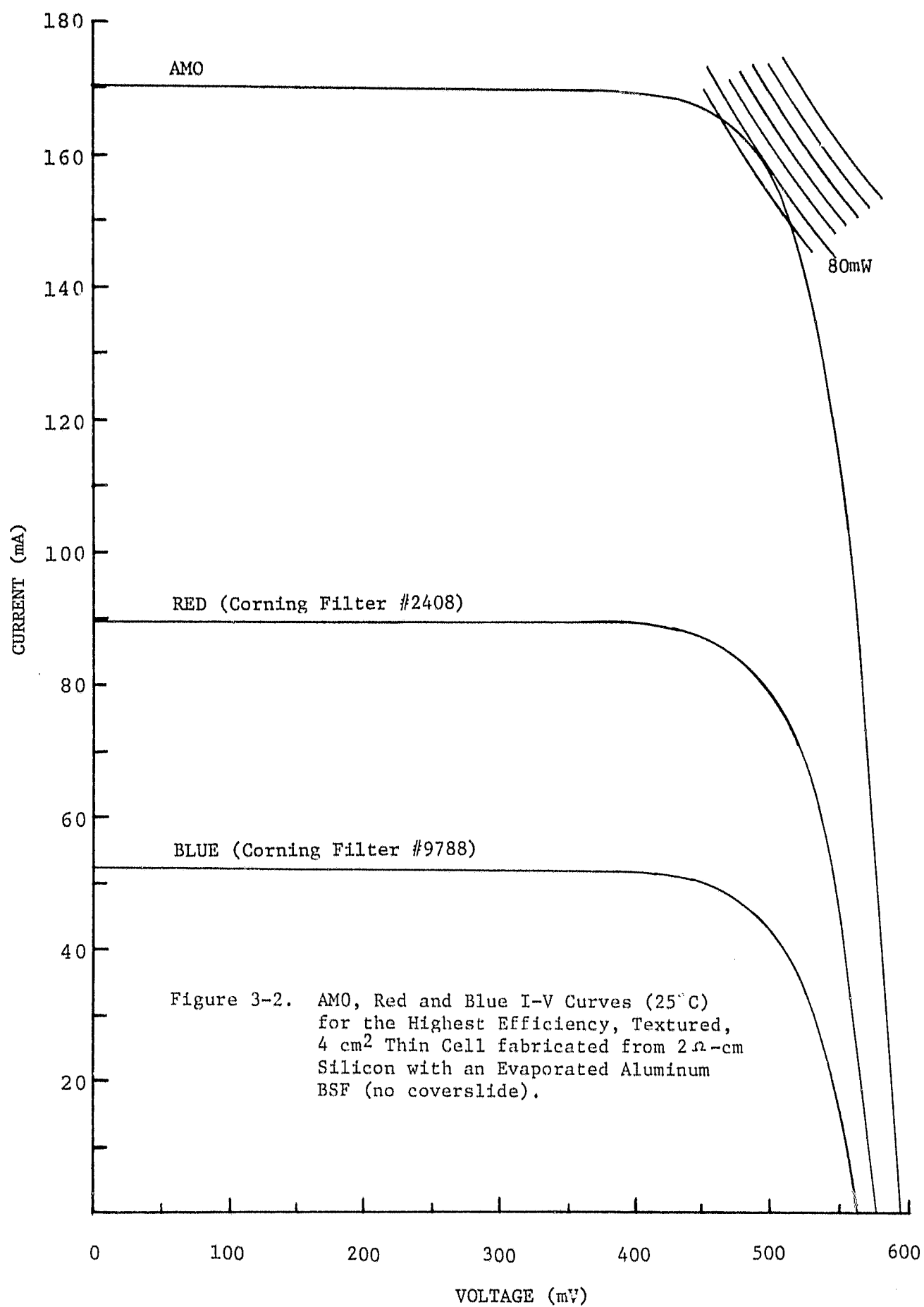
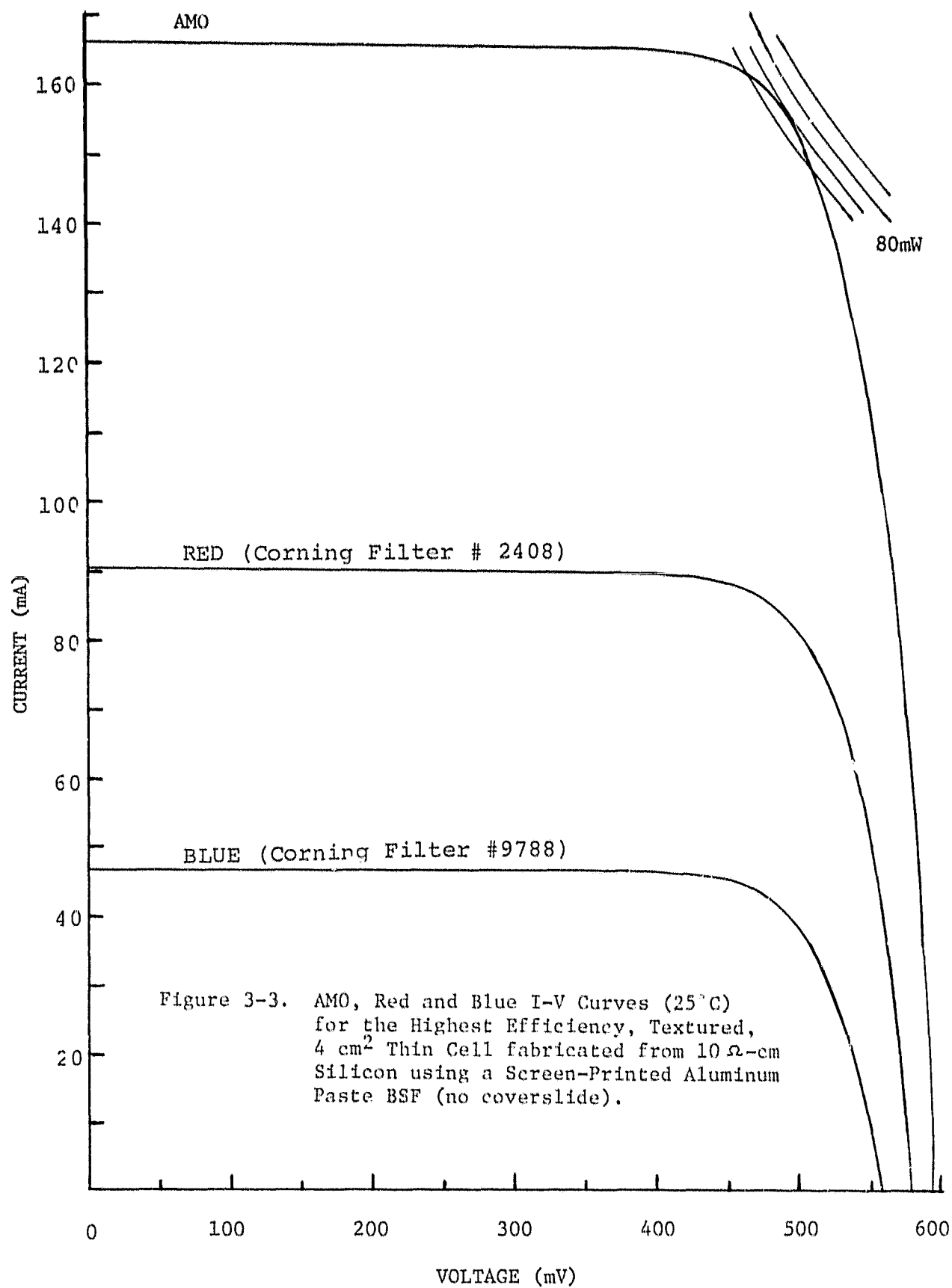


Figure 3-2. AMO, Red and Blue I-V Curves (25°C) for the Highest Efficiency, Textured, 4 cm² Thin Cell fabricated from 2 Ω -cm Silicon with an Evaporated Aluminum BSF (no coverslide).



Some cells were also fabricated from 2 Ω -cm material, and the highest efficiency cells were obtained in this effort. The cell characteristics are seen in Figure 3-4. The power density of the cell was 20.3 mW/cm² (15% AMO) with a J_{sc} of 42.3 mA/cm² and a V_{oc} of 607 mV.

The above cells were all fabricated with processes that are readily transferable to a pilot line operation. It is expected that cells having efficiencies approaching these levels are achievable in pilot line production runs.*

A relatively limited effort was expended in attempting to improve the efficiency of 25 cm² ultra-thin cells. The best cell (using a textured surface) fabricated in this effort had a power density of 16.4 mW/cm², a current density of 37.2 mA/cm², and a V_{oc} of 572 mV.

Table 3-1 summarizes the data on these high-efficiency cells. Values of open-circuit voltage, short-circuit current density, output power, and conversion efficiency are for AM0 illumination at 25°C. This data shows that by the fifth quarter of this contract a 4 cm² cell of relatively high base resistivity material could be fabricated with an

*Note: It should be pointed out that the pilot line run of 4 cm² cells did not utilize textured surfaces at the request of Jet Propulsion Laboratory.

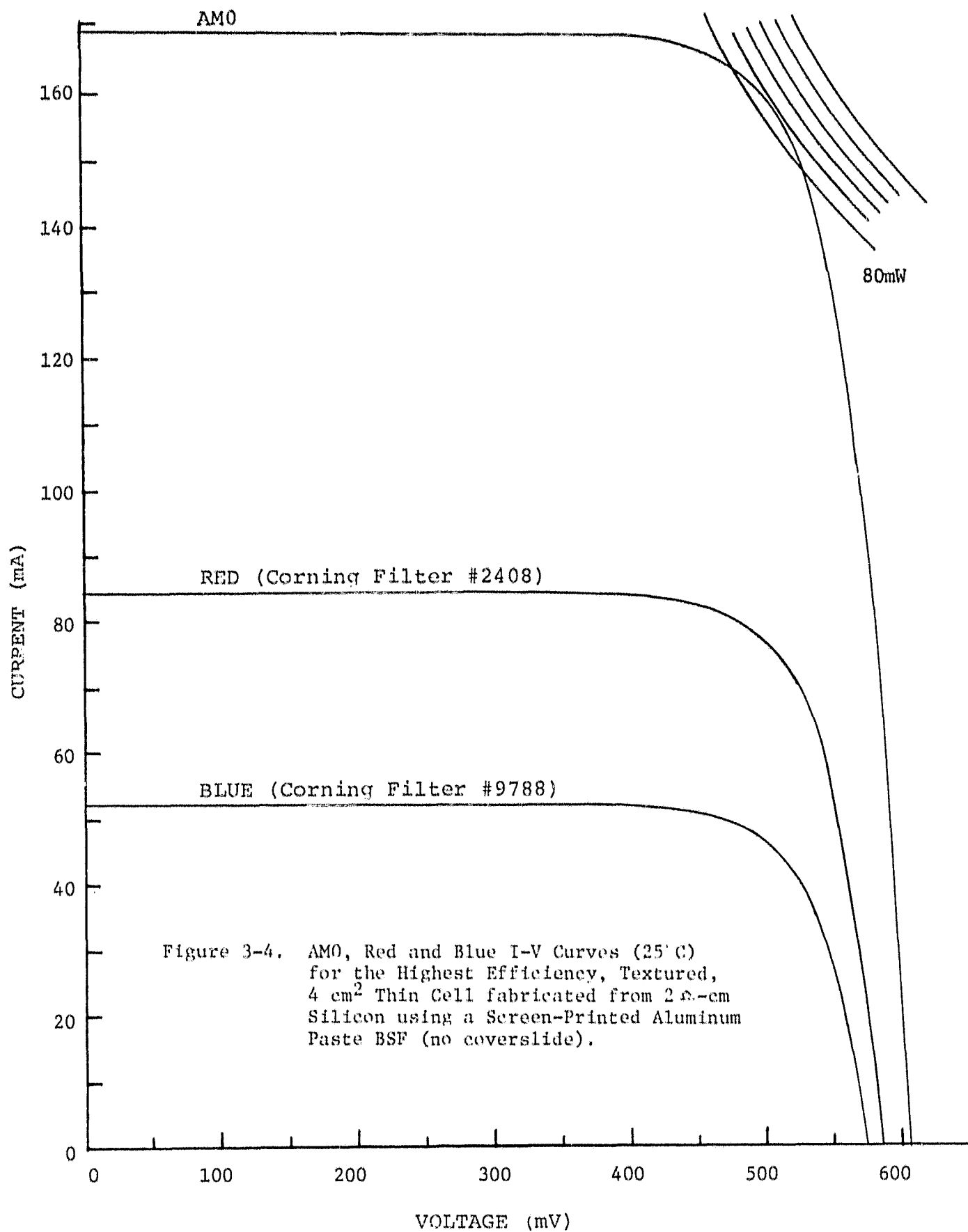


Table 3-1.

Highest Efficiency, Textured, 50 μm Thick Cells
AMO, 25°C

Cell Technology	V_{OC} (mV)	J_{SC} (mA/cm ²)	P (mW/cm ²)	η (%)
2 Ω -cm, evaporated BSF, 4 cm ² 2nd quarter	565	41.8	18.3	13.5
2 Ω -cm, evaporated BSF, 4 cm ² 4th quarter	594	42.5	19.9	14.7
10 Ω -cm, paste BSF, 4 cm ² 5th quarter	595	41.5	19.3	14.3
2 Ω -cm, paste BSF, 4 cm ² 8th quarter	607	42.3	20.3	15.0
10 Ω -cm, paste BSF, 25 cm ² 7th quarter	572	37.2	16.4	12.1

AMO efficiency which is nearly as high as the efficiency of a cell made from 2 Ω -cm silicon with an evaporated aluminum BSF. This development was achieved by incorporating an aluminum paste BSF and improved alloy residue clean-up techniques into the process. Optimization of these techniques ultimately led to the fabrication of a 15% efficient, 50 μ m thick cell from 2 Ω -cm silicon in the eighth quarter. The best large area (25 cm²) ultra-thin cell was fabricated from 2 Ω -cm silicon with a paste BSF and had an AMO conversion efficiency of 12.1%.

4. Pilot Line Experience

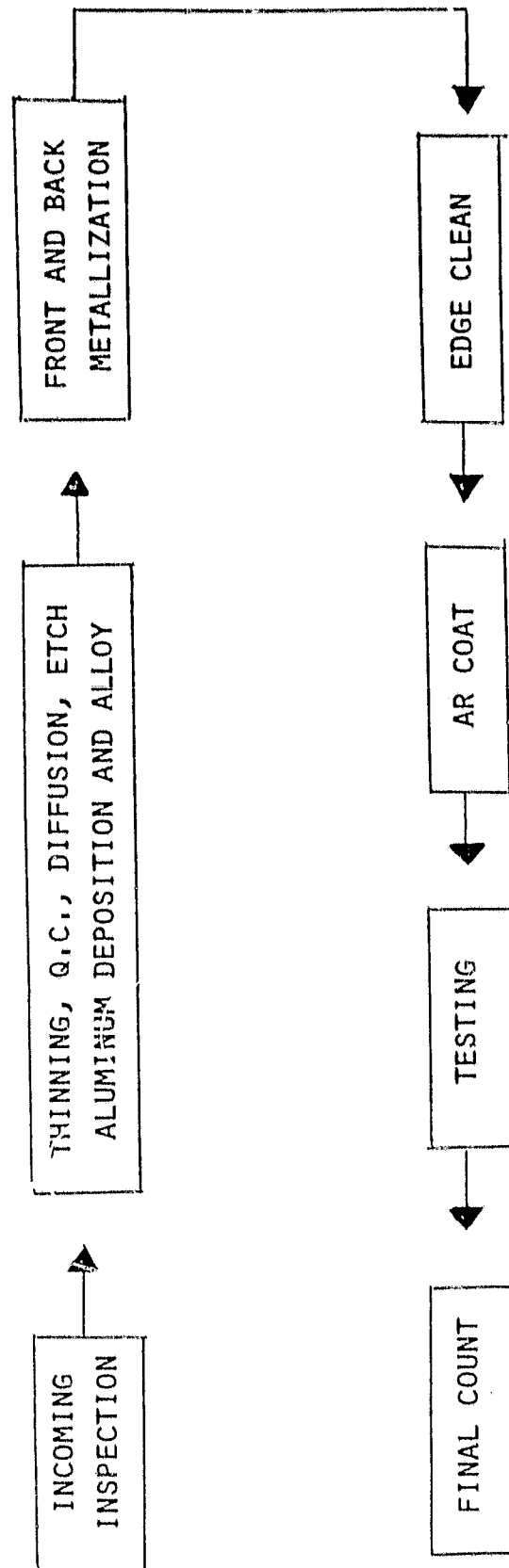
Since the focus of this contract was directed toward actually fabricating 5,000, 2 cm x 2 cm ultra-thin cells over the first four quarters, and 2,000, 2 cm x 2 cm ultra-thin cells plus 1,000 5 cm x 5 cm ultra-thin cells in the tenth quarter, the results of the work leading up to these operations can best be evaluated in light of the pilot line experiences. We summarize here the results obtained in producing both small and large-area ultra-thin cells. Detailed experience and results are covered in separate Pilot Line Reports (see references 3 and 5) also issued as part of this contract. A summary of the ultra-thin cell processing is included as an Appendix to this report.

4.1 2 cm x 2 cm Pilot Line operated over Quarters 1 to 4

4.1.1 Processes and Procedures

Figure 4-1 shows the process sequence for cells produced by the 2 cm x 2 cm Pilot Line which operated over the first four quarters of this contract. For the most part, the processes are identical to those used in the first ultra-thin cell pilot line (JPL Contract No. 954290). However, a significant improvement in conversion efficiency was obtained by modifying the diffusion and alloy processes.

PROCESS SEQUENCE DIAGRAM



EACH STEP HAS ACCURATE ACCOUNTING AND LOSS MODE RECORD FOR ALL PROCESS LGTS.

Figure 4-1

As in the first pilot line effort, the wafers were 2 Ω -cm p-type, boron doped, Czochralski-grown silicon, etched to a 50 μm thickness by means of a two-step NaOH etch. The BSF was formed by alloying 7000 \AA , rather than 5000 \AA , of evaporated aluminum at a temperature of 850°C or 900°C for 15 or 10 minutes, respectively. During this pilot line wafers were tilted in angled-slot diffusion boats, so that the front was convex-stressed during the diffusion process, a utilization of results from experimental work. Stressed wafers were diffused with phosphine at 850° for 15 minutes to a sheet resistivity of 100 - 120 Ω/\square . During the latter part of this pilot line, the BSF alloy residues were removed by etching in HCl, followed by rinsing the wafers in an ultrasonic DI water bath. This gave more consistent results with respect to output power. Front contacts were Ti/Pd/Ag fabricated by the photolithographic masking technique. Evaporated Ta_2O_5 was used as the AR coating; the cells were sintered at 450° for 45 seconds.

The following procedure was used to assure the mechanical quality of the cells. First, the front contact of each cell was inspected to determine that less than 5% of the contact fingers were missing, that there was no evidence of contact bubbling or peeling, and that no busses or fingers had lifted. The rear contact was inspected to determine that silver had plated to more than 90% of the rear contact area and that

there was no evidence of rear contact peeling or bubbling. The cells were inspected to determine that the cell area was within 0.5% of the nominal area.

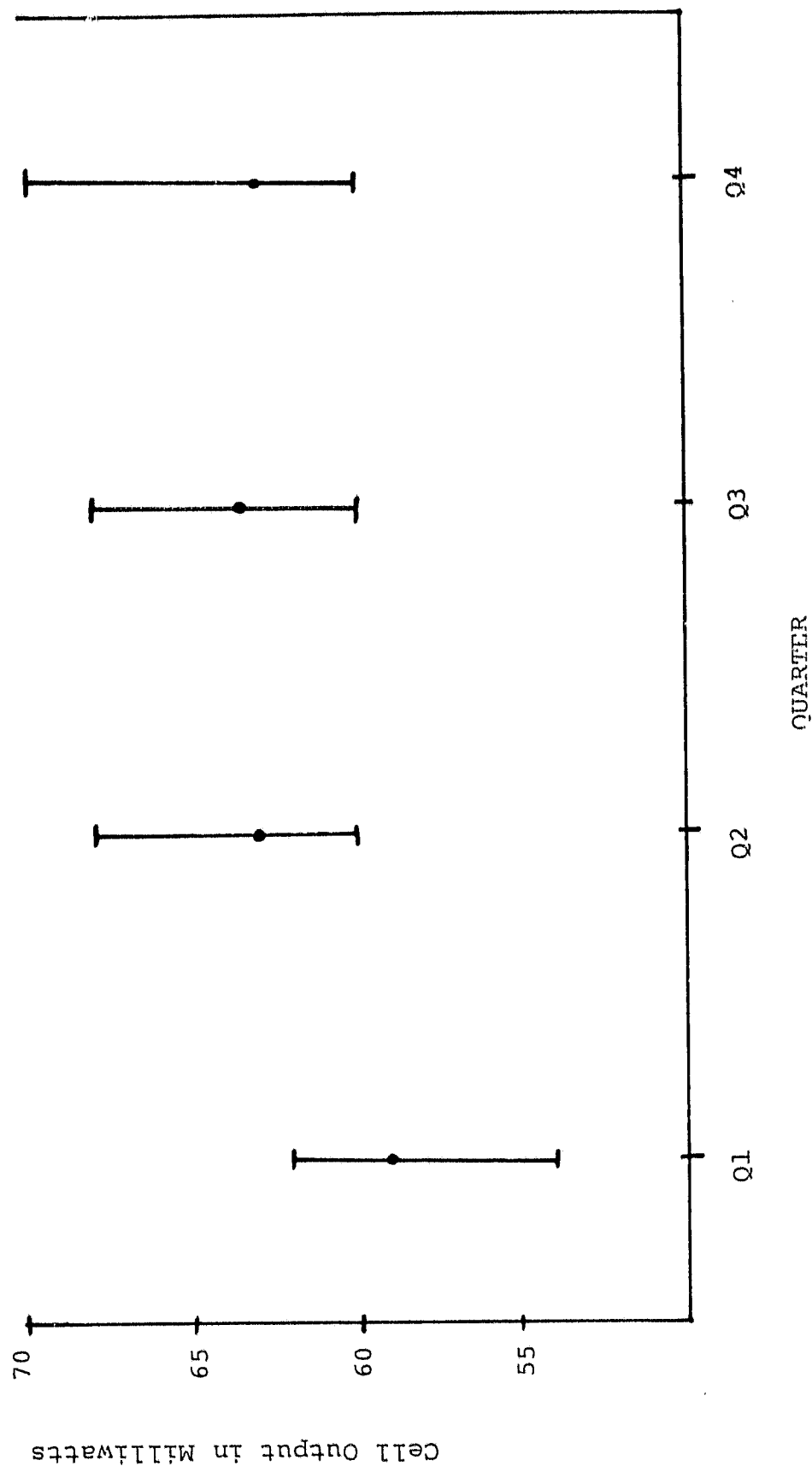
The electrical performance of the cells was measured using a xenon simulator calibrated by reference cells. The minimum specification for power output was 60 mW for AM0 illumination at 25°C.

4.1.2 Results

A significant improvement in conversion efficiency was obtained in this pilot line after the first quarter due to diffusion of wafers with their front surfaces convex-stressed. This can be seen in Figure 4-2 which shows a plot of output power versus quarter. Each of the first three quarters rep-

Figure 4-2. TYPICAL CELL POWER AT AMO

(The minimum, average and maximum values are all averages of the values of each lot).



resents results from 1,000 cells and the last quarter, 2,000 cells. The average output power increased from 59 mW in the first quarter to better than 63 mW in the second, third, and fourth quarters.

A total of 27,516 cells was started in order to ship 5,000 deliverable cells. Yields for all four quarters were low (not exceeding 35% for any quarter). The overall pilot line yield of 26% is lower than that of the first pilot line, a result of the start-stop nature of the operation, and in the third quarter, to high personnel turnover. However, a production rate of 10,000 cells per month was demonstrated.

The major source of loss (31% of starts) was due to front contact metallization failure. Although it was not clear why so many cells had bad contacts, the contacts were characteristically either sound and well bonded to the cells, or catastrophically weak. Another source of loss was handling breakage. Loss due to breakage decreased from 20% (of starts) in the first quarter to only 16% (of starts) in the second. However, high personnel turnover in the third quarter caused handling breakage to increase to more than 26% (of starts). During the fourth quarter, when over 10,000 cells were started, less than 22% were lost due to breakage. Hence, it was shown that handling breakage is related to operator experience and would be reduced with steady full-rate operation.

4.1.3 Discussion

Operation of this pilot line effort demonstrated that high efficiency (>11.5% at AMO, 25°C) ultra-thin (50 μm thick) cells could be fabricated at a production rate of 10,000 cells per month with existing equipment (assuming a yield of 50% is maintained in steady productions). The average AMO power output increased from 59 mW in the first quarter to 63 mW in the third, mainly due to modification of the diffusion process to purposely stress the wafer during diffusion. Better cleanup of the alloy residues also improved performance and reduced losses due to back contact failure. It was shown that higher throughput in the etch thinning, metal evaporation, and AR coating processes would be necessary to readily operate at the 10,000 cells per month rate. Also, it was determined that two areas were most in need of improvement -- front contact adhesion and operator handling breakage.

4.2 Final 2 cm x 2 cm Pilot Line - Tenth Quarter

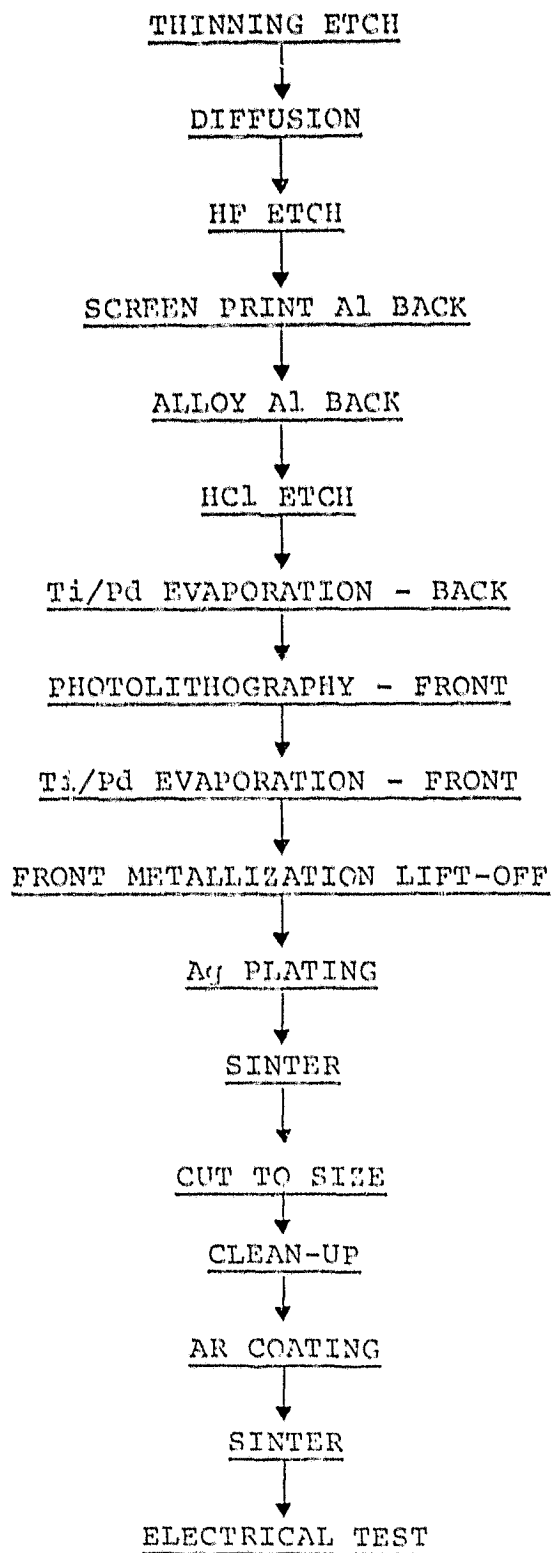
4.2.1 Processes and Procedures

The culmination of the research and development efforts to improve the performance and fabrication of ultra-thin cells in the latter part of this contract was the operation of two pilot lines, one to produce 2 cm x 2 cm cells and one to produce

large-area, 5 cm x 5 cm cells. These pilot lines were substantially different from the previous pilot lines in that ultra-thin cells were to be fabricated with screen-printed aluminum paste alloyed back surface fields. This technique has been shown to yield superior results with respect to performance when compared to evaporated aluminum BSF's in small experimental lots. The purpose of the 2 cm x 2 cm pilot line effort was to demonstrate that incorporation of the screen-printed aluminum paste BSF would improve cell performance, even in the relatively high bulk resistivity (7-14 Ω -cm) material, without sacrificing yields.

A flow chart of the processes used in the 2 cm x 2 cm ultra-thin cell pilot line is shown in Figure 4-3. The starting material was 7 to 14 Ω -cm, p-type, boron doped, Czochralski silicon. The wafers were etched to a thickness of 50 μ m by a two-step NaOH etch process. Thinned wafers were phosphorous diffused to approximately 100 Ω/\square , then etched in HF to remove the diffusion glass. The diffused wafers were printed with Englehard A3484 aluminum paste, baked at 220°C for 20 minutes, then alloyed at 850°C for 25 seconds. The unalloyed aluminum was removed using an HCl etch, and any oxides were stripped by a quick HF etch. Ti/Pd was then evaporated onto this back surface. Front contact metallization was accomplished using Ti/Pd evaporated onto a pattern defined by photolithography. Excess metal was removed using an acetone lift-off bath. Approximately 9 to 10 μ m of silver were then electroplated onto the Ti/Pd

Figure 4-3. 2 cm x 2 cm Process Diagram



conductors. After sintering the metallizations, the wafers were cut into 2 cm x 2 cm cells, which were subsequently cleaned in a methanol bath. A Ta_2O_5 AR coating was evaporated and sintered at 475°C for about 30 seconds. Completed cells were then tested with an Xenon simulator calibrated by reference cells. The minimum specification for output power was 60 mW with AM0 illumination at 25°C . The criteria for mechanical quality used in the previous pilot line were used in this effort.

A more detailed description of the processes and procedures can be found in the Appendix.

4.2.2 Results

Incorporation of the screen-printed aluminum paste alloyed BSF resulted in a significant improvement in output power, when compared to pilot line cells fabricated with evaporated aluminum BSF's. The best quarterly average power for cells fabricated in the previous pilot line was 63 mW (third quarter). Pilot line cells fabricated in the tenth quarter with aluminum paste BSF's had an average output power of over 67 mW. Many cells had an AM0 output power of greater than 70 mW, and very few had an output power of less than 60 mW.

The overall yield of this pilot line (AM0 power output at 25°C greater than 60 mW) improved substantially as experience in handling the 50 μm thick cells was gained. The best yield was over 51%, and the average for the five lots of the pilot line was better than 38%.

Most of the losses were due to handling breakage (31% of starts) followed by front contact failure (14% of starts) and breakage in the spin dryers (5% of starts). Unlike the losses due to front contact failures and spin-dryer breakage which remained fairly constant, handling breakage decreased from 42% of starts in the first lot to less than half that value in the fourth lot, indicating the significance of operator experience in reducing handling breakage.

Since the integrity of the front contact metallization is essential for good operation of the cells, and since there were a substantial number of front contact failures in the previous pilot line effort, tape peel tests were performed (using the standard technique) on thick cells which were processed together with the ultra-thin cell lots. The average failure rate (where a failure meant that more than 5% of the contact fingers were pulled off) was 4.3%, but there were very few or no failures in three out of five lots. To further test front contact integrity, electrical or mechanical reject ultra-thin cells were tested by the tape peel test (after sticking them to a flat surface). Very few cells (typically less than 2%) failed the test indicating that, if fingers were not visibly lifting, the contacts had good adherence.

4.2.3 Discussion

Operation of this pilot line successfully demonstrated that a significant improvement in performance of ultra-thin cells could be

achieved by use of an aluminum paste BSF without sacrificing yield. Incorporation of the screen-printed BSF did not impact the yield for several reasons. Losses due to breakage by the screen-printer were negligible as a result of redesigning the screen-printer chuck to hold the wafer more gently and securely. In earlier small production runs, loss due to breakage in the post-alloy HCl etch could be as high as 30%, mainly as a result of stress from the alloy process. However, during this pilot line effort breakage at the post-alloy etch was reduced to less than 5% of starts by adjusting the screen-printer to produce thinner paste layers and less warped wafers after alloy. Finally, at the photo-resist spin-on step, the wafers were cushioned on the spinner chuck by a plastic film which minimized the effects of lumps left from the BSF alloy.

Very few cells were broken during silver plating (less than 3% of starts). This indicates that our efforts to redesign the plating racks to improve the wafer hold-down were successful.

When compared to the previous pilot line, this pilot line achieved a substantial improvement in the integrity of the front contact. In the earlier effort, over 31% of the cell starts were rejected due to front contact failure. In this operation, the front contact failure loss was reduced to 14% of starts. This result was due to several changes in wafer processing at the photolithographic, metal evaporation, and plating steps. First, a previously used HF etch

step after photolithographic pattern development and prior to the front Ti/Pd evaporation was omitted. Removal of the thin room-temperature oxide between the metallization and the front surface is unnecessary since sintering provides good electrical contact through the oxide. Second, increased exposure time improved adhesion (but at the expense of some increase in shadowing). And finally, introduction of a low temperature heat treatment (150° for 20 minutes) after the front Ti/Pd evaporation and prior to silver plating resulted in better contact integrity.

As mentioned previously, the overall yield of this pilot line was better than 38%, and the best lot yield was over 51%. It was shown, by using the best yield at each process step, that the overall yield could be increased to 70% if the personnel and pilot line were experienced and if the existing equipment and processes were optimized. Further improvement in ultra-thin cell fabricability and yield could be obtained by developing more controlled and gentler wet-processing steps.

4.3 5 cm x 5 cm Pilot Line - Tenth Quarter

4.3.1 Processes and Procedures

A second pilot line was operated in the tenth quarter in order to investigate large-scale production of large area (25 cm²) ultra-thin cells. Pilot line processing of these cells was in many aspects identical to those utilized in the tenth quarter of 2 cm x 2 cm pilot line. However, since a large number of losses were anticipated in

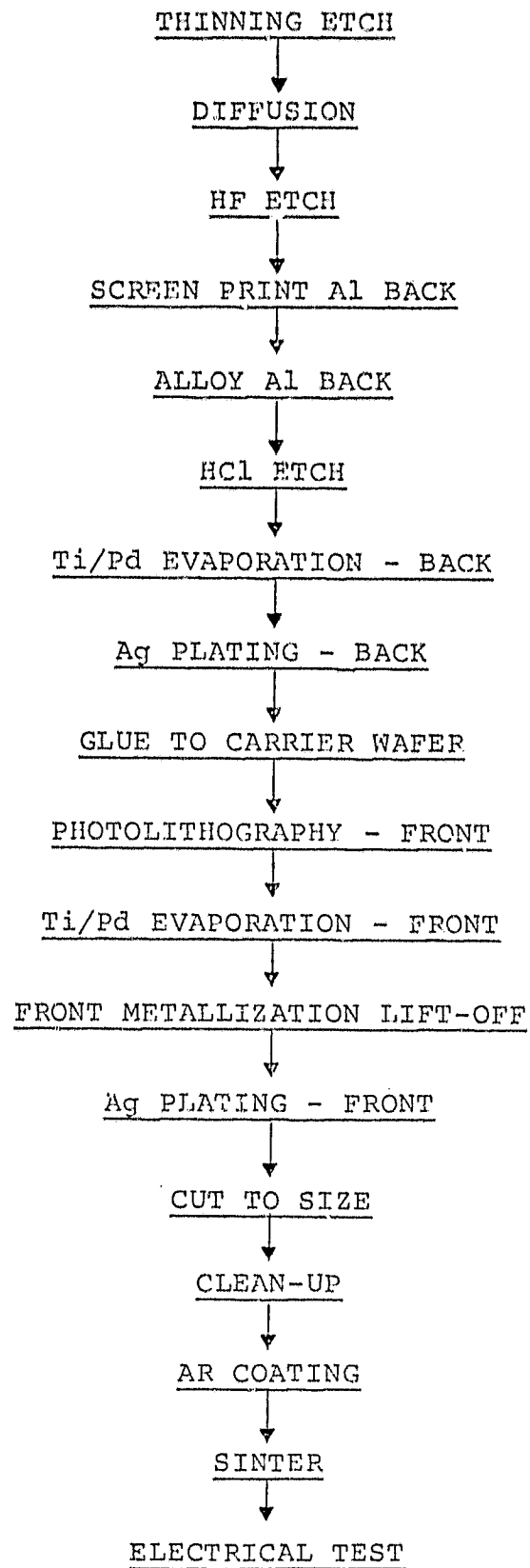
the later process steps, the 50 μm thick wafers were attached to thick carrier wafers using cyanoacrylate adhesive after the back contact Ti/Pd evaporation and silver plating. The wafers were therefore reinforced during the photolithography, front Ti/Pd evaporation and silver plating, and cutting steps. The cyanoacrylate adhesive was chosen because it decomposes at approximately 300°C and, therefore, wafers or cells could be readily removed from the reinforcing carrier during a sinter operation. A flow chart of the 5 cm x 5 cm Pilot Line is shown in Figure 4-4. The same criteria for mechanical quality used in previous pilot lines applied to this effort. The minimum specification for output power was 338 mW with AM0 illumination at 25°C.

4.3.2 Results

The results from the first operation of a large area (25 cm²), ultra-thin cell pilot line were encouraging. The average AM0 output power (at 25°C) for the pilot line effort was better than 387 mW. The lot average increased from 372 mW in the first lot to more than 392 mW in the third lot.

While the overall yield of this pilot line (AM0 power output at 25°C greater than 338 mW) was low, approximately 13%, it did show substantial improvement as experience was gained. The lot yield increased from only 7% in the first lot to better than 17% at the end of this effort. The majority of the losses (62%) were due to handling breakage, particularly at the thinning etch, back plating and post-alloy etch. Only the attrition at the post-alloy etch showed a significant reduction with experience. Losses

Figure 4-4. 5 cm x 5 cm Process Diagram



due to breakage at all other processes were constant. Very few cells (6% of starts) were rejected due to failure of the front contact metallization, even if plating rejects are included (13% of starts).

4.3.3 Discussion

This pilot line operation demonstrated that large area (25 cm^2) ultra-thin cells could be fabricated with low, but not unreasonable, yields since this was the first attempt at pilot line production of large area ultra-thin cells. In fact, the lot yields consistently improved as experience in handling the large area cells was gained. This is important since most of the losses were due to handling breakage. As with the previous 2 cm x 2 cm pilot line, utilization of an aluminum paste BSF was not found to impact the yield with respect to breakage, but it did result in an average AMO output power of better than 387 mW.

Losses due to front contact failure were the same or lower than those experienced in the previous 2 cm x 2 cm pilot line. This is consistent since similar processing techniques were utilized in the tenth-quarter pilot lines.

Since this was a first pilot line attempt with large area ultra-thin cells, further significant improvements in yield can be expected simply from processing experience, mainly because handling breakage was the major mode of loss.

5. Conclusions and Recommendations

Utilization of an aluminum paste back surface field, together with modification of several processes and techniques, has resulted in ultra-thin (50 μm thick) cells which are light weight, have high efficiency, are more resistant to radiation, and can be produced with good yield using existing technology.

Work performed under this contract has shown that the optimum aluminum paste back surface field is formed by screen-printing a layer (1 to 2 mils thick) of aluminum paste, baking the paste to drive off the volatile solvents, and then rapidly alloying the dried paste at 800°C to 850°C. The efficacy of the aluminum paste BSF was demonstrated by the exercise of a pilot line in the tenth quarter which produced 4 cm^2 ultra-thin cells from relatively high bulk resistivity (7-14 $\Omega\text{-cm}$) silicon with an average AM0 conversion efficiency of 12.4%. This should be contrasted to an earlier pilot line in which 4 cm^2 ultra-thin cells were fabricated from 2 $\Omega\text{-cm}$ silicon with evaporated aluminum BSF's. In that particular effort, the best lot average AM0 conversion efficiency was only 11.6% .

Surface texturing was not detrimental to ultra-thin cell performance. Texturing of the front surface was found to increase the absorptance without degrading the open-circuit voltage. Back surface texturing appeared to result in more consistent for-

mation of a BSF. The best 4 cm² ultra-thin cell was fabricated from textured 2 Ω -cm silicon with an aluminum paste BSF and had an AMO conversion efficiency of 15%.

The performance of ultra-thin cells is sensitive to high-temperature stress during diffusion and alloy. Significant improvements in output power are possible by convex-stressing the fronts, as shown by the increase from the first to the third quarter pilot lines.

High efficiency, ultra-thin cells can be fabricated at a production rate of 10,000 cells per month using existing equipment and technologies. The process of screen-printing an aluminum paste BSF does not inherently result in a significant reduction in yield due to breakage. Instead, the yield of this process is strongly dependent on the amount of stress applied to the wafer by the solidification of the excess (non-alloyed) aluminum. Breakage was minimized when the aluminum paste was printed with 200 or 250 mesh screens. Wafers which were printed with lower mesh screens (150 or 100) had thicker paste layers, were more stressed after alloy, and experienced significantly more breakage during the alloy residue clean-up process.

This program has shown that high efficiency in ultra-thin silicon solar cells can be produced with good yield

using existing technology and processes. However, additional development work is required to obtain satisfactory yields on 25 cm² cells.

Further improvements in ultra-thin cell performance and fabrication could be achieved by incorporating the following recommendations:

1. A back surface reflector should be incorporated in order to increase efficiency.
2. Further optimization of the back surface field formation is required in order that higher open-circuit voltages are obtained with high yields.
3. Additional development work is required on the 25 cm² ultra-thin cells in order to increase yields. Specifically, process steps should be investigated that will result in reduced breakage.

Appendix: Ultra-Thin Cell Processing

1. Wafer Thinning

1.1 Wafer Sorting

- (a) Sort wafers into 7 μ m groups (e.g., $300 \pm 3.5\mu$ m).

1.2 Wafer Etching

- (a) Place sorted wafers into Teflon cassettes.
- (b) Etch wafers in a solution of 30% (by weight) NaOH in water at 110°C to a thickness of 100 to 120 μ m. (Calculate etch time using an etch rate of 15 μ m/min).
- (c) Stop the etching in a water bath; measure the wafer thickness and calculate the real etch rate to determine the amount of time needed to achieve the required thickness.
- (d) Return cassette to etch bath; to stop the etch, place the cassette into a stop bath of tap water as quickly as possible.

1.3 Thinning Etch Residue Clean-up

- (a) Rinse in water.
- (b) Rinse in a solution of HCl and DI water.
- (c) Rinse in water.
- (d) Rinse in DI water to 7M Ω resistivity.
- (e) Spin dry.

2. Diffusion

- (a) Set diffusion tube temperature to 850°C.
- (b) Load boat with wafers.
- (c) Load boat into diffusion tube with an Ar purge; continue to purge while moving boat slowly into the center zone.
- (d) Dope wafer with PH₃-Ar, O₂ and Ar.
- (e) Flush the tube with O₂ and Ar.
- (f) Unload boat from diffusion tube.

3. BSF Formation

3.1 Diffusion Glass Removal

- (a) Remove phosphosilicate glass with an HF and water etch.
- (b) Rinse in DI water to 7M Ω resistivity.

3.2 Al Paste Screen-printing

- (a) Screen-print 1 to 2 mils of Englehard A3484 aluminum paste.
- (b) Bake wafers at 220°C for 20 minutes to drive off the volatile solvents.

3.3 Alloy

- (a) Set alloy tube temperature at 850°C.
- (b) Load wafers into boats with paste side up.
- (c) Load and unload wafers from tube very quickly; alloy wafers in the center zone for approximately 25 seconds.

3.4 Alloy Residue Clean-up

- (a) Place wafers in cassettes.
- (b) Etch in HCl until effervescence stops.
- (c) Rinse in water.
- (d) Rinse in DI water to 7M Ω resistivity.
- (e) Spin dry.

4. Back Metallization Evaporation

4.1 Load wafers into evaporator.

4.2 Pump down system to 2×10^{-5} Torr.

4.3 Evaporate Ti/Pd metals.

- (a) 450 Å Ti.
- (b) 450 Å Pd.

4.3 Vent system and unload wafers.

5. Photolithography

5.1 Resist spinning

- (a) Prebake wafers at 90°C for 20 minutes.
- (b) Spin on Hunt 204 photoresist at 3500 rpm for 15 seconds.
- (c) Bake at 90°C for 20 minutes.

5.2 Expose pattern

5.3 Develop pattern

- (a) Develop.
- (b) Rinse in water.
- (c) Spin dry.

6. Front Metallization Evaporation

6.1 Load wafers into evaporator.

6.2 Pump down system to 2×10^{-5} Torr,

6.3 Evaporate Ti/Pd metals.

- (a) 450 Å Ti.
- (b) 450 Å Pd.

6.4 Vent system and unload wafers.

7. Front Metallization Lift-Off

7.1 Metallization Lift-off

- (a) Soak in acetone to loosen resist.
- (b) Wipe wafers to remove resist and excess metal.
- (c) Rinse in acetone.
- (d) Rinse in isopropanol.
- (e) Rinse in water.
- (f) Spin dry.

8. Silver Plating

8.1 Rack and Wafer Preparation

- (a) Bake wafers at 150°C for 20 minutes.
- (b) Attach wafers to racks with magnet hold downs.

8.2 Plate Wafers

8.3 Silver-plating Clean-up

- (a) Remove wafers from racks and place in cassettes.
- (b) Rinse in water.
- (c) Rinse in DI water to 7M Ω resistivity.
- (d) Spin dry.

9. Cutting

9.1 Sinter wafers for 15 seconds at 475°C.

9.2 Cut wafers into cells.

9.3 Cutting Residue Clean-up

- (a) Rinse in acetone.
- (b) Rinse in isopropanol.
- (c) Rinse in water.
- (d) Rinse in DI to 7 M Ω resistivity.

10. Anti-Reflection Coating

10.1 Mount cells on holders and load into the evaporator.

10.2 Pump down system to 2×10^{-5} Torr.

10.3 Evaporate approximately 700 Å of Ta₂O₅.

11. Sintering

11.1 Sinter cells at 475°C for 30 seconds.

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